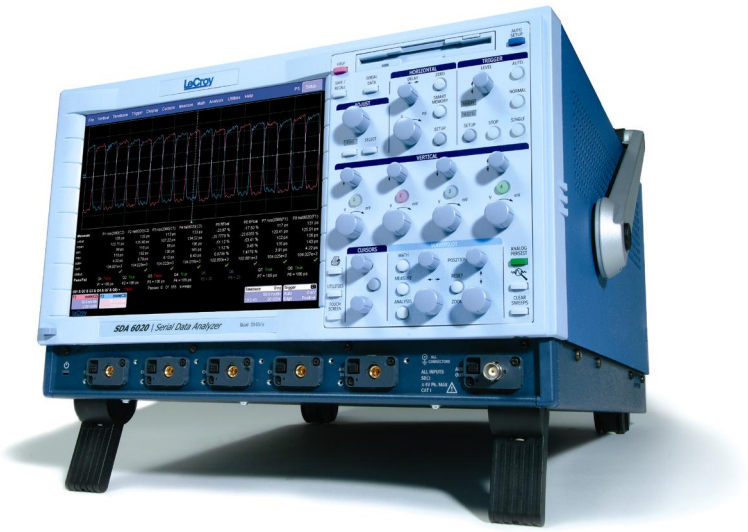
LeCroy

SDA-SATA
Software Option Package

PHY Common MOI Template

Version 1.0



Operator's Manual

February 2006

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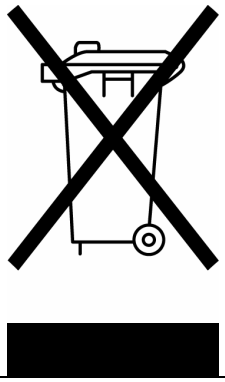

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SDA-SATA-OM-E Rev C
913978 Rev A

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INTRODUCTION

SDA-SATA is a software package designed to capture, analyze, and report measurements in conformance with Serial ATA II electrical specification standards. A current copy of the specification can be found at www.serialata.org

Member, SATA-IO Logo Task Force (LTF)

The LeCroy SDA-SATA software manual has been updated to refer to specific sections of the PHY MOI (methods of implementation) manual.

LeCroy PHY MOI

For SDA-11000 v1.0.1

Derived from SATA Logo Program

PHY Common MOI Template

Version 1.0

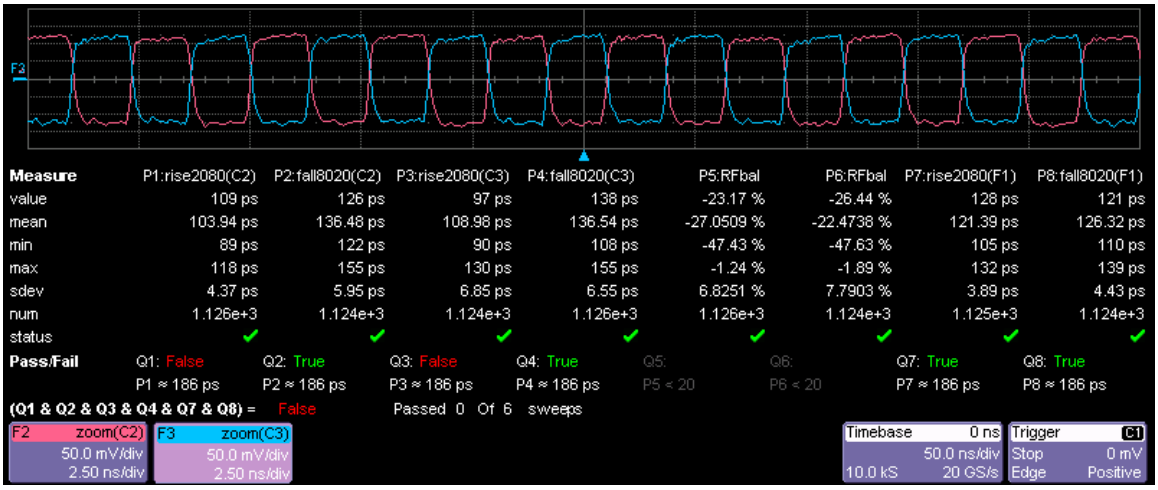
Technical Document

SATAii has two speeds (Gen1 and Gen2) and at each speed there are three different configurations or Usage modes:

- i = internal
- m = "Short" Backplane and External Desktop Applications
- x = Extended, system to system.

SDA-SATA consists of separate VBS files for Gen1i, Gen1m, Gen1x, Gen2i, Gen2m, and Gen2x. In all cases, a report is generated giving the test results from each of the six scripts. In addition there are a few scripts to set up the user interface on the SDA.

There is a separate VBS script for each of the six flavors of SATAii. The scripts specify setup files to recall, and save results for report generation.



Compatibility

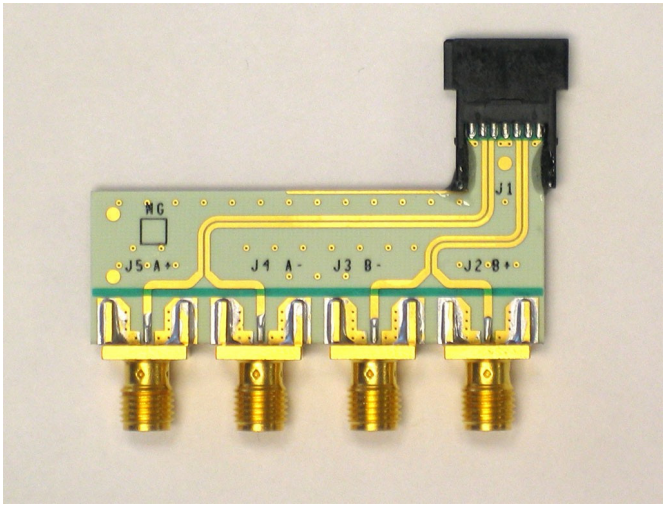
SDA-SATA is a software option that is compatible with the following LeCroy X-Stream oscilloscopes:

- SDA 6000, 6000A (4x10 GS/s, 2x20 GS/s)
- SDA 6020 (4x20 GS/s)
- SDA 11000 (4x20 GS/s at 6 GHz bandwidth, 2x40 GS/s at 11 GHz bandwidth)

Because the SATA specification for Gen1 and Gen2 data rate is 1.5 Gb/s and 3 Gb/s, respectively, oscilloscope bandwidths less than 4 GHz for Gen1 and 6 GHz for Gen2, therefore, are not recommended. The SATA specification requires at least 10 GHz bandwidth for certain measurements.

SATA Test Fixture

Test fixtures are required to connect the signal under test to the oscilloscope running the SDA-SATA software. The fixtures are available from LeCroy (part number TF-SATA) and consist of the test fixture and two 30-inch cables with SMA connectors. They provide a means to probe the device under test via a standard SMA connector interface. The same fixture is compatible with both Gen1 and Gen 2 SATA standards.



The use of this fixture for measuring each standard is described in the respective sections of this manual.

SETUP AND INSTALLATION

Equipment Required

The following test equipment is required to perform SATA tests:

- Real Time Digital Oscilloscope: LeCroy SDA 6000A, SDA 6020, or SDA 11000, with firmware release 4.0.2.0 or later, and software option package ASDA-J Advanced Serial Data Analysis.
- 50-ohm Coax Cable with SMA Male Connectors, qty=2 (supplied with test fixture)
- LeCroy Serial ATA Test Fixture: TF-SATA
- Serial ATA cable (not supplied)
- Device Under Test: Disk drive or other device equipped with SATA-approved connector

Recommended Equipment for SATA Compliant Signal Generation

LeCroy recommends the use of a Serial ATA compliant Protocol Analyzer / Bus Exerciser to communicate SATA compliant messages to a device under test (DUT) in accordance with the standard. See LeCroy's Technical Brief describing the use of such equipment to activate and configure a DUT by issuing BIST activate FIS.

- LeCroy Universal Protocol Analysis System (UPAS) model 10000 configured with the following modules:

  - SAS/SATA Analyzer Model SAS 001MA

  - SAS/SATA Exerciser Model SAS 001MG

- Host Computer with SAS Tracer/Trainer Version 1.3 or later software loaded, and USB2 interface

Installing SDA-SATA Software in the Oscilloscope

- Existing SDA+ASDA users: Load the SDA-SATA applications software CD and follow these installation instructions:

  1. Insert the SDA-SATA CD in the disk drive. Windows should automatically detect the presence of the CD.
  2. The SATA Installer should start automatically. If it does not, double-click **SATAiiInstaller.exe**. The installation process will now begin with the Installation Wizard. Click **Next** to Continue.
  3. Select **Components to install**. All components (SATA Test Suite, SASTracer Scripts and SIGTEST support) are checked by default. SASTracer script files need to be installed in the computer that will serve as host to the Protocol Analyzer/Exerciser.
  4. If prompted for a destination directory for SASTracer scripts, enter a directory, or the files will be written to C:\Program Files\CATC\SASTracer\Scripts
  5. Click the **Install** button to proceed with installation.
  6. The SATA scripts will be installed in D:\Applications\SATAii.
  7. If D: drive is not available, the Installer will install the SATA scripts and setups in c:\program files\lecroy\sataii
  8. When installation is complete, click **Finish** to close the Installation Wizard

- For New SDA+ASDA users: when equipment is configured with the ASDA option key, there is no additional software installation required. SDA-SATA is already installed.

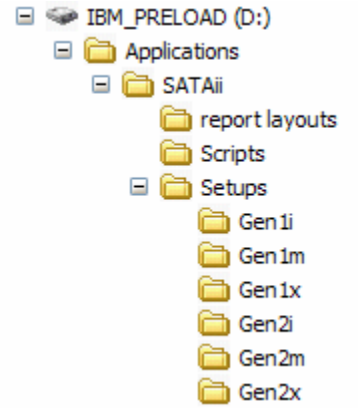


Fig 1: Directory tree for SATA scripts and setup files

- The following software files are installed in **D:\Applications\SATAii\Scripts**:

  Gen1iJitter.lss
  Gen1iScript.lss
  Gen1mScript.lss
  Gen1xJitter.lss
  Gen1xScript.lss
  Gen2iJitter.lss
  Gen2iScript.lss
  Gen2mScript.lss
  Gen2xJitter.lss
  Gen2xScript.lss
  SetupGen1.lss
  SetupGen2.lss
  Close.lss

- The following setup files are installed in D**:\Applications\SATAii\Setups\Gen1i**:

  SATAiiGen1iAmplHFTP.lss
  SATAiiGen1iJitter.lss
  SATAiiGen1iNoSSCFreqHFTP.lss
  SATAiiGen1iSSCFreqHFTP.lss
  SATAiiGen1iTiming.lss
  SATAiiGen1iVdiffMaxLFTP.lss
  SATAiiGen1iVdiffMaxMFTP.lss
  SATAiiGen1iVdiffMinHFTP.lss
  SATAiiGen1iVdiffMinLBP.lss
  SATAiiGen1iVdiffMinMFTP.lss

- The following setup files are installed in **D:\Applications\SATAii\Setups\Gen1m**:

  SATAiiGen1mVdiffMinHFTP.lss
  SATAiiGen1mVdiffMinLBP.lss
  SATAiiGen1mVdiffMinMFTP.lss

- The following setup files are installed in **D:\Applications\SATAii\Setups\Gen1x**:

  SATAiiGen1xAmplHFTP.lss

SATAiiGen1xJitter.lss

SATAiiGen1xNoSSCFreqHFTP.lss

SATAiiGen1xSSCFreqHFTP.lss

SATAiiGen1xTiming.lss

SATAiiGen1xVdiffMaxLFTP.lss

SATAiiGen1xVdiffMaxMFTP.lss

SATAiiGen1xVdiffMinHFTP.lss

SATAiiGen1xVdiffMinLBP.lss

SATAiiGen1xVdiffMinMFTP.lss

- The following setup files are installed in **D:\Applications\SATAii\Setups\Gen2i**:

  SATAiiGen2iAmplHFTP.lss

  SATAiiGen2iJitter.lss

  SATAiiGen2iNoSSCFreqHFTP.lss

  SATAiiGen2iSSCFreqHFTP.lss

  SATAiiGen2iTiming.lss

  SATAiiGen2iVdiffMaxLFTP.lss

  SATAiiGen2iVdiffMaxMFTP.lss

  SATAiiGen2iVdiffMinHFTP.lss

  SATAiiGen2iVdiffMinLBP.lss

  SATAiiGen2iVdiffMinMFTP.lss

- The following setup files are installed in **D:\Applications\SATAii\Setups\Gen2m**:

  SATAiiGen2mVdiffMinHFTP.lss

  SATAiiGen2mVdiffMinLBP.lss

  SATAiiGen2mVdiffMinMFTP.lss

- The following setup files are installed in **D:\Applications\SATAii\Setups\Gen2x**:

  SATAiiGen2xAmplHFTP.lss

  SATAiiGen2xJitter.lss

  SATAiiGen2xNoSSCFreqHFTP.lss

  SATAiiGen2xSSCFreqHFTP.lss

  SATAiiGen2xTiming.lss

  SATAiiGen2xVdiffMaxLFTP.lss

  SATAiiGen2xVdiffMaxMFTP.lss

  SATAiiGen2xVdiffMinHFTP.lss

  SATAiiGen2xVdiffMinLBP.lss

  SATAiiGen2xVdiffMinMFTP.lss

Several other helper files are installed in D:\Applications\SATAii\Setups.

- The following software files are installed in **D:\XPort**

  SATAGen2xReportLayout.xslt

  SATAGen1iJitterReportLayout.xslt

  SATAGen1iReportLayout.xslt

  SATAGen1xJitterReportLayout.xslt

  SATAGen1xReportLayout.xslt

  SATAGen2iJitterReportLayout.xslt

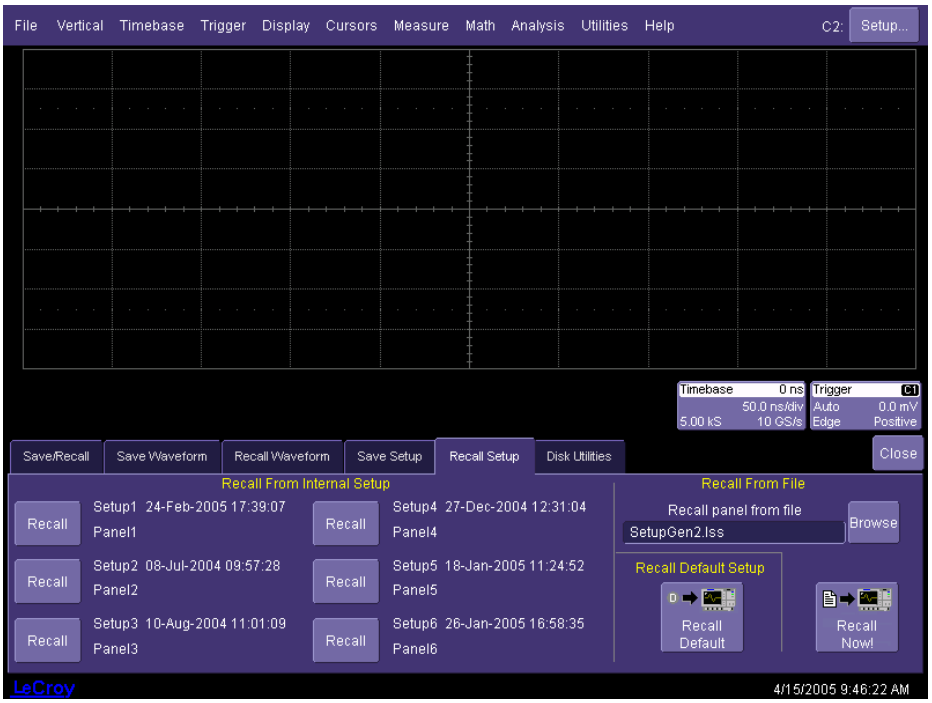
  SATAGen2iReportLayout.xslt

  SATAGen2xJitterReportLayout.xslt

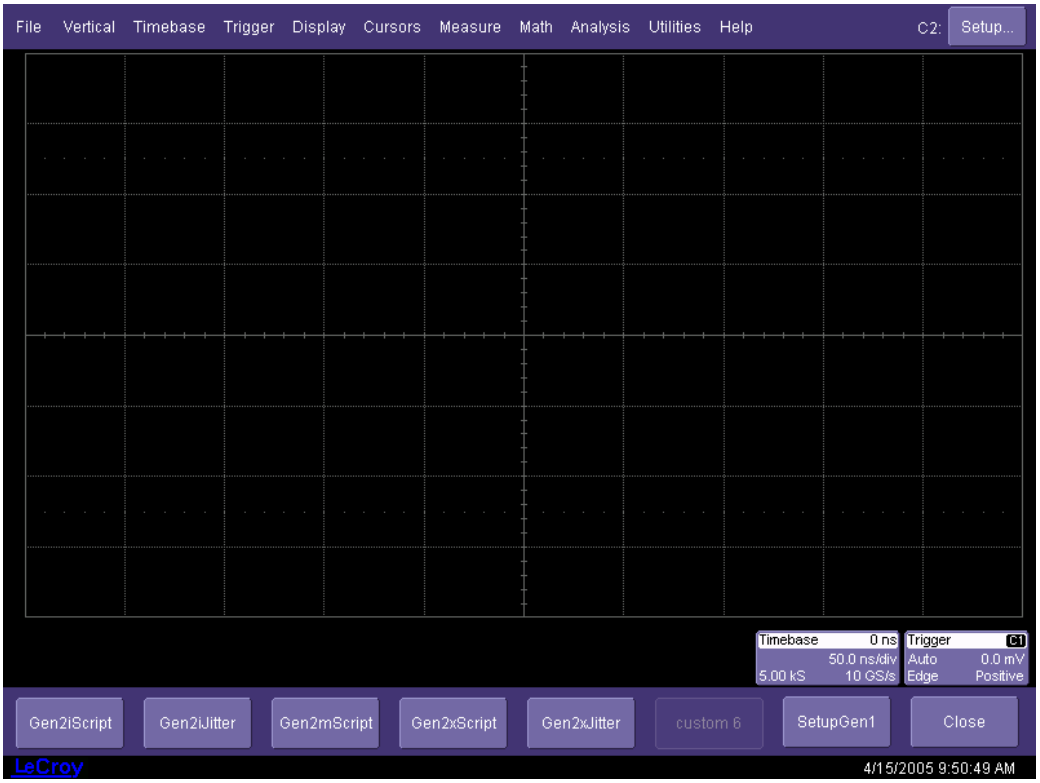
Configuring Custom DSO to Execute Scripts

To use these tests:

1. Ensure that all the files are installed in their correct locations (see previous section).
2. From the SDA menu bar, select **File**, then **Recall Setup...** from the drop-down menu. Browse to **D:\Applications\SATAii\Scripts** and then select either SetupGen1.lss or SetupGen2.lss, and recall that setup. This sets up the SDA's CustomDSO feature for you, ready to run all the scripts appropriate for Gen1 or Gen2.



3. After recalling SetupGen1.lss or SetupGen2.lss, the scope should look like the following figure, which shows the result of SetupGen2.lss selection.



4. The title for each of the scripts selected will appear inside each of the action buttons for which scripts were associated. Unused buttons will appear greyed out.

   Now the software is ready to run SATA tests. Next, a very important step when using differential signal pairs as the input waveform: deskewing the signal pairs for accurate timing and amplitude alignment (see next section).

5. If inputs are not deskewed, proceed to the next section before running the scripts. Otherwise, press the button associated with the selected script and follow instructions on the screen for test pattern connection and SSC mode selection, etc.

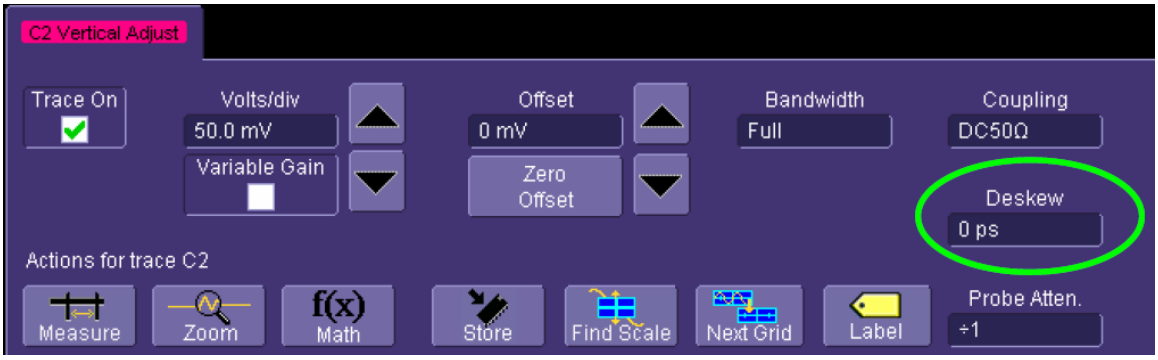
Input Signal Deskew Test Procedure

First, the two scope channels utilized for the tests (C2 and C3) must be deskewed:

1. Using a SATA device as the signal source, connect an SMA cable from B+ on the TF-SATA to C2, and another from B- on the TF-SATA to C3.
2. On an SDA 6000A or SDA 11000, select **Timebase** from the menu bar, then **Horizontal Setup…** from the drop-down menu. Set Active Channels to 2 on the SDA 6000A and 11 GHz mode on the SDA 11000. Set the Time/Division to 50 ns.
3. Set the Trigger Mode to Auto. Adjust the voltage scale and offset of C2 and C3 and the trigger level as appropriate.
4. From the menu bar, select **Measure Setup...**
5. Set up P1 as **Skew** (C2,C3) with slope = **Both** for “Skew Clock1” and “Skew Clock 2”. In the “Measure” dialog, check **Statistics On**. Record the mean value. The screen will look something like this:

6. Swap the two cables. Now the cable that had been connected from B+ to C2 should be connected from B- to C3 and vice-versa.
7. Press Clear Sweeps on the front panel or from **Measure Setup…**
8. Record the mean value.
   The first measured skew value is: device skew + cable skew.
   The second measured skew value is: device skew - cable skew.

   Subtract the second mean value from the first mean value. The result is twice the cable skew. Divide the result by two to obtain the deskew value.
9. Select **Vertical** from the menu bar, then **Channel 3 Setup…** from the drop-down menu. Select **Deskew** and enter the derived deskew value. The skew measurement should now be approximately half-way between the 2 measured skew values.



Test Pattern Generation Using LeCroy SATA/SAS Tracer/Trainer

HFTP = High Frequency Test Pattern

MFTP = Medium Frequency Test Pattern

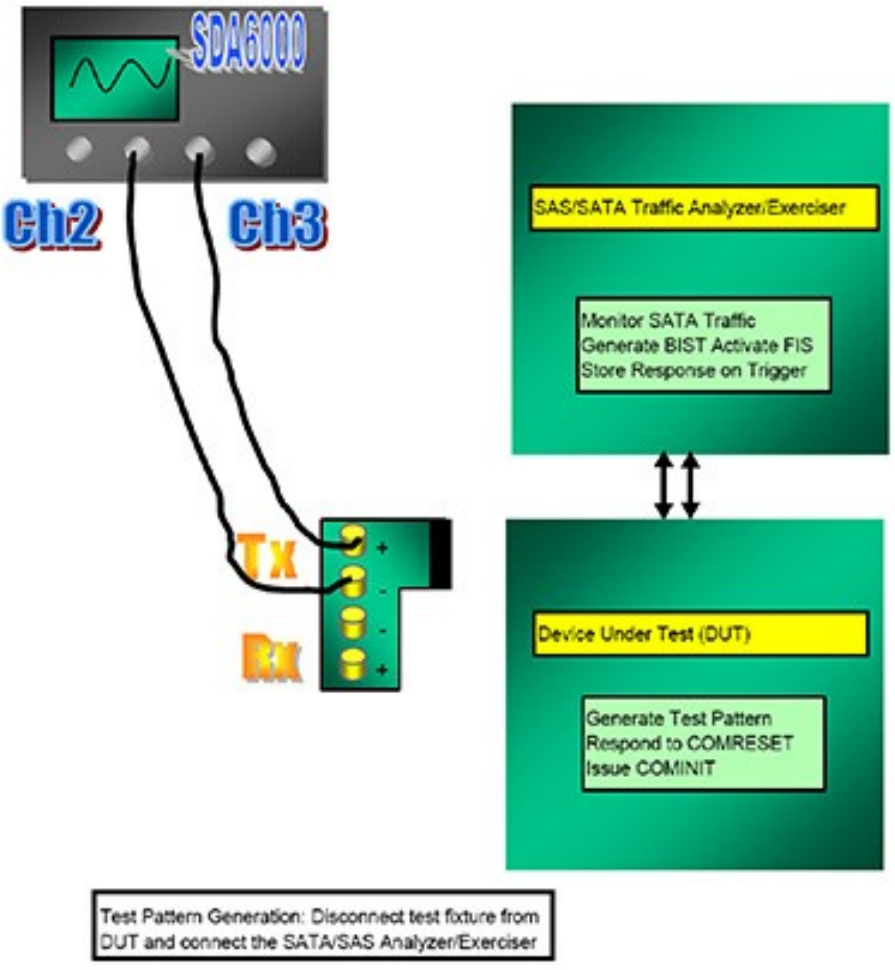
LFTP = Low Frequency Test Pattern

LBP = Lone Bit Pattern

SSOP = Simultaneous Switching Outputs Pattern

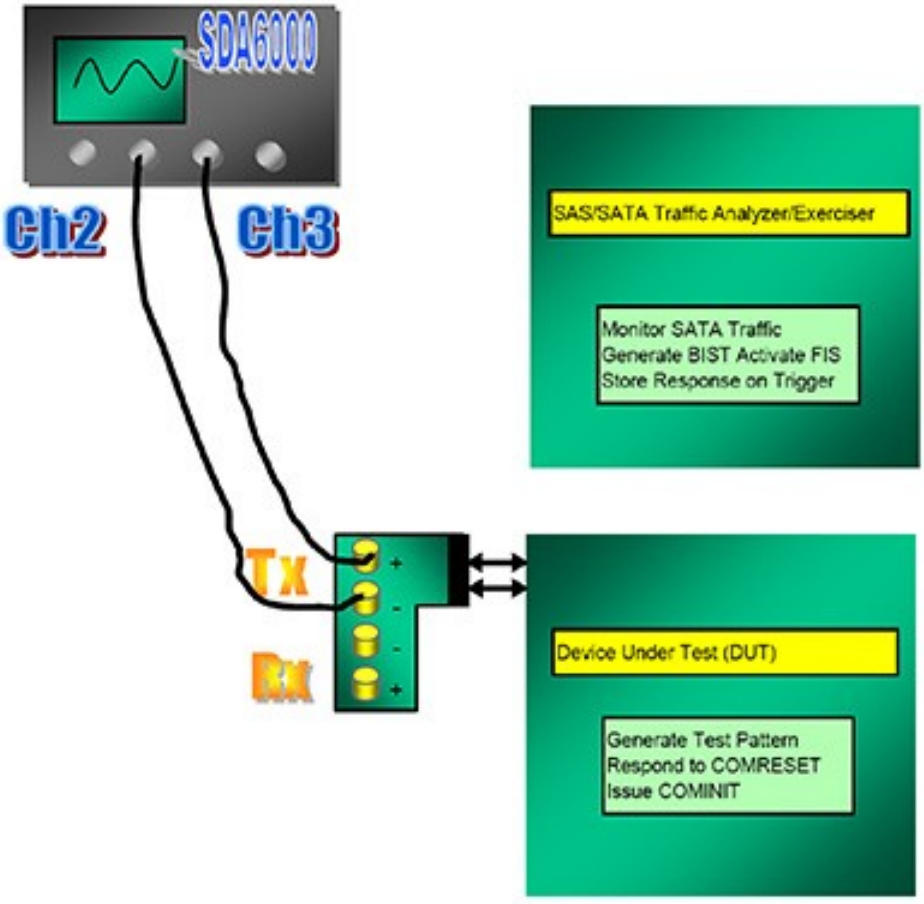
Running the SATA test scripts requires the generation of test patterns to determine DUT compliance to SATA specifications. Any method that causes the DUT to produce the required patterns is acceptable. LeCroy uses a Protocol Analysis solution to exercise DUT test patterns. LeCroy's SASTracer software allows you to load individual scripts to cause the Host (in this case, the SATA emulator) to initiate SATA traffic. These scripts use BIST Activate FIS; the DUT must be able to respond to BIST Activate. The following section describes the specific actions required to successfully generate test patterns from a DUT connected to LeCroy SATA/SAS Tracer/Trainer. It is assumed that you have started SASTracer/Trainer software in the host computer and established communication with the Tracer/Trainer instrument via USB. When you are prompted to generate a specific test pattern during the execution of a SATA script, the requested pattern can be created by using the following steps:

1. Connect SATA device cable between the DUT and the output LeCroy Pattern Analyzer ("To Target") port. The SATA test fixture will remain disconnected, as shown in the following figure:



Load the GenFile for the desired test pattern. There are generation files (*.ssg) included for each of the required SATA device test patterns. There are separate files for regular devices as well as ATAPI devices and for 1.5 Gb/s as well as 3 Gb/s devices. By default these files are installed in "C:\Program Files\CATC\SASTracer\Scripts\BIST"

2. Configure Bus Analyzer to start acquisition/trigger on event: SATA FIS → BIST Activate.
3. Start recording, then press **Start Generation**, which will trigger the bus analyzer to record data upon issue of BIST activate FIS. At this point, the DUT is generating a test pattern as specified in the traffic generation file.
4. Disconnect SATA cable from Device Under Test and connect SATA test fixture to the scope via SMA cables and directly into the DUT.



DUT Compliance Test: Disconnect Traffic Exerciser and connect DUT to SATA Test Fixture, as shown

5. These SATA exerciser scripts have been verified to work on production disk drives from several companies. However, not all devices respond to BIST Activate even though it is required by the SATA specification.

Test Descriptions and Reference

As shown in the above test setup, it is recommended to use a SATA Host to initiate the DUT by issuing OOB signaling (COMRESET) and also to set up the applicable FIS (BIST Activate) required to exercise the DUT for SATA compliance.

LeCroy uses a LeCroy SATA/SAS Traffic Exerciser/Analyzer to generate test patterns. SDA-SATA software is supplied with the required Traffic Generation Scripts in order to use the Exerciser portion of the SAS/SATA

analyzer and issue a BIST (Built In Self Test). Activate FIS in order for the DUT to issue test patterns required to measure electrical compliance to SATA standards.

For jitter scripts, however, longer patterns are needed that cannot be specified with BIST, so it is up to the user to determine how to generate correct jitter test patterns. The specific implementation varies from device to device.

Important Note: All the scripts described in this section can be edited to generate other results. Any modifications to the scripts are made at the exclusive risk of the user. LeCroy is not responsible for changes made by users that modify the expected behavior or produce software or equipment malfunctions.

New for Release 1.2 of SDA-SATA Scripts: Differential Skew

MOI Reference: TSG-03

Test Procedure:

Differential Skew is reported for HFTP and separately (near the end of the report) for MFTP. Either "Pass" or "FAIL" is shown for each. TSG-03 passes only if both results, Differential Skew for HFTP and for MFTP, pass.

Observable Results:

The TX Differential Skew shall be between the limits specified in reference [1]. For convenience, the values are reproduced below.

Device Type	Max Diff Skew
Gen1i, Gen1m, Gen1x	20 ps
Gen2i, Gen2m	20 ps
Gen2x	15 ps

Gen 1 Tests

Gen1i Test

Unit Interval (UI) and SSC Frequency Tolerance tests

	MOI Reference	Test Criteria
Tui min:	PHY-01 - Unit Interval	>/= 666.4333 ps
Tui max:	PHY-01 - Unit Interval	</= 670.2333 ps
ftol:	PHY-02 – Frequency Long Term Stability	1.5 GHz ±525 kHz
fssc:	PHY-03 - Spread-Spectrum Modulation Frequency	30-33KHz

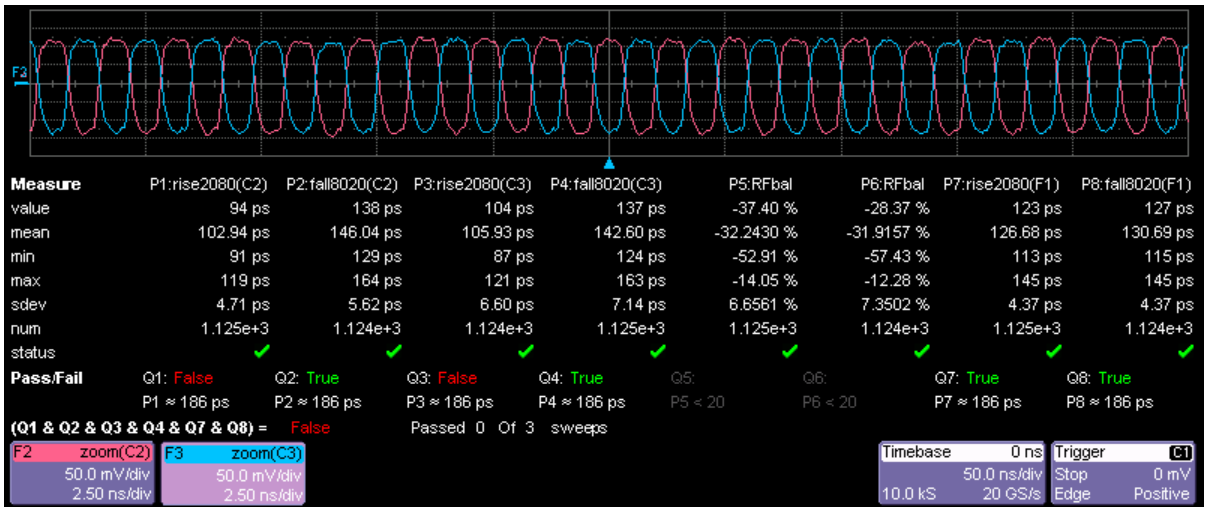
- Rise and Fall Times

	MOI Reference	Test Criteria
t2080 + rise:	Not in IL Test Report	100 ps to 273 ps
t2080 + fall:	Not in IL Test Report	100 ps to 273 ps
t2080 - rise:	Not in IL Test Report	100 ps to 273 ps
t2080 - fall:	Not in IL Test Report	100 ps to 273 ps
t2080 differential Rise:	TSG-02 - Rise/Fall Time	100 ps to 273 ps
t2080 differential Fall:	TSG-02 - Rise/Fall Time	100 ps to 273 ps

- Vdiff min, max Tests

	MOI Reference	Test Criteria
DH (Vdiff min HFTP):	TSG-01- Differential Output Voltage	> 400 mV
DM (Vdiff min MFTP):	TSG-01- Differential Output Voltage	> 400 mV
VtestLBP (Vdiff min LBP):	TSG-01- Differential Output Voltage	> 400 mV
pu (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pl (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pu (Vdiff max LFTP):	TSG-01- Differential Output Voltage	< 0.05
pl (Vdiff max LFTP):	TSG-01- Differential Output Voltage	< 0.05

Example: Gen 1i Rise & Fall Times, RF Balance

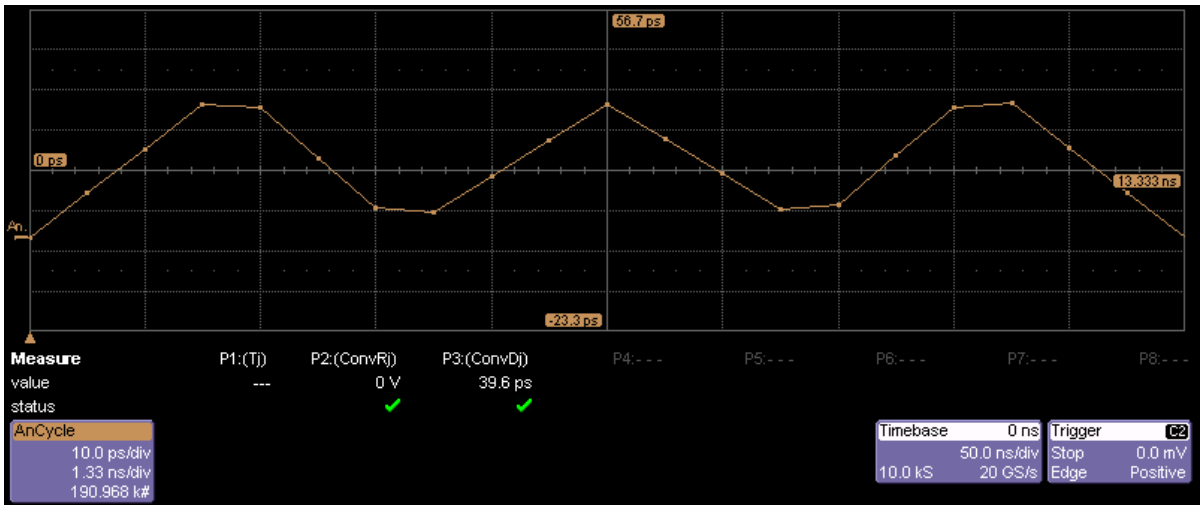


Gen 1i Jitter Tests

- Jitter, Data-Data, 5UI (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
TJ:	TSG-07 - TJ at Connector, Data, 5UI	< 236.667 ps
DJ:	TSG-08 - DJ at Connector, Data, 5UI	< 116.667 ps

Example: Edge to Edge Jitter, 5UI



	limit
TJ:	313.333 ps
DJ:	146.333 ps

Gen1m Tests

- Tui, ftol, fssc (if SSC is present); HFTP (Ref # 6.2.1 Table 2 - General Specifications)

	MOI Reference	Test Criteria
Tui min:	PHY-01 - Unit Interval	>/= 666.4333 ps
Tui max:	PHY-01 - Unit Interval	</= 670.2333 ps
ftol:	PHY-02 – Frequency Long Term Stability	1.5 GHz ±525 kHz
fssc:	PHY-03 - Spread-Spectrum Modulation Frequency	

- Rise and Fall Times, High Frequency Test Pattern: t20-80TX, HFTP (Ref #6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
t2080 + rise:	Not in IL Test Report	100 ps to 273 ps
t2080 + fall:	Not in IL Test Report	100 ps to 273 ps
t2080 - rise:	Not in IL Test Report	100 ps to 273 ps
t2080 - fall:	Not in IL Test Report	100 ps to 273 ps
t2080 differential Rise:	TSG-02 - Rise/Fall Time	100 ps to 273 ps
t2080 differential Fall:	TSG-02 - Rise/Fall Time	100 ps to 273 ps

- Vdiff min, max tests (Ref #6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
DH (Vdiff min HFTP):	TSG-01- Differential Output Voltage	> 400 mV
DM (Vdiff min MFTP):	TSG-01- Differential Output Voltage	> 400 mV
VtestLBP (Vdiff min LBP):	TSG-01- Differential Output Voltage	> 400 mV
pu (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pl (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pu (Vdiff max LFTP):	TSG-01- Differential Output Voltage	< 0.05
pl (Vdiff max LFTP):	TSG-01- Differential Output Voltage	< 0.05

Every item must pass for VdiffTX to be considered passed. Items are labeled as in 6.4.4 of the spec, with a note in parentheses telling what is being tested.

Note: These tests require 10 GHz of bandwidth. Results obtained with 6 GHz of bandwidth must be regarded as an indicator and not the true compliance test.

- Parameters tested: Rise and Fall Times with Medium Frequency Test Pattern, t20-80TX, R/F balance; MFTP (6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	limit
t2080 + rise:	Not in IL Test Report	100 ps to 273 ps
t2080 + fall:	Not in IL Test Report	100 ps to 273 ps
t2080 - rise:	Not in IL Test Report	100 ps to 273 ps
t2080 - fall:	Not in IL Test Report	100 ps to 273 ps
t2080 differential Rise:	TSG-02 - Rise/Fall Time	100 ps to 273 ps
t2080 differential Fall:	TSG-02 - Rise/Fall Time	100 ps to 273 ps

Gen1x Tests

- Amplitude balance, HFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
AmpBal max:	TSG-06 - Amplitude Imbalance	within 10%
AmpBal min:	TSG-06 - Amplitude Imbalance	within 10%

- Tui, ftol, fssc (if SSC is present); HFTP (Ref# 6.2.1 Table 2 - General Specifications)

	MOI Reference	Test Criteria
Tui min:	PHY-01 - Unit Interval	>/= 666.4333 ps
Tui max:	PHY-01 - Unit Interval	</= 670.2333 ps
ftol:	PHY-02 – Frequency Long Term Stability	1.5 GHz ±525 kHz
fssc:	PHY-03 - Spread-Spectrum Modulation Frequency	

- t20-80TX, R/F bal; HFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
t2080 + rise:	Not in IL Test Report	67 ps to 273 ps
t2080 + fall:	Not in IL Test Report	67 ps to 273 ps
t2080 - rise:	Not in IL Test Report	67 ps to 273 ps
t2080 - fall:	Not in IL Test Report	67 ps to 273 ps
t2080 differential Rise:	TSG-02 - Rise/Fall Time	67 ps to 273 ps
t2080 differential Fall:	TSG-02 - Rise/Fall Time	67 ps to 273 ps

- Vdiff min, max tests (6.2.1 Table 4 - Transmitted Signal Requirements)

  Every item must pass for VdiffTX to be considered passed. Items are labeled as in 6.4.4 of the spec, with a note in parentheses telling what is being tested.

- Measurement of DH, Vdiff min for HFTP (see Spec Ref # 6.4.4 for test description)

	MOI Reference	Test Criteria
DH (Vdiff min HFTP):	TSG-01- Differential Output Voltage	> 400 mV
DM (Vdiff min MFTP):	TSG-01- Differential Output Voltage	> 400 mV
VtestLBP (Vdiff min LBP):	TSG-01- Differential Output Voltage	> 400 mV
pu (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pl (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pu (Vdiff max LFTP):	TSG-01- Differential Output Voltage	< 0.05
pl (Vdiff max LFTP):	TSG-01- Differential Output Voltage	< 0.05

- Amplitude balance and Vcm-ac, MFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

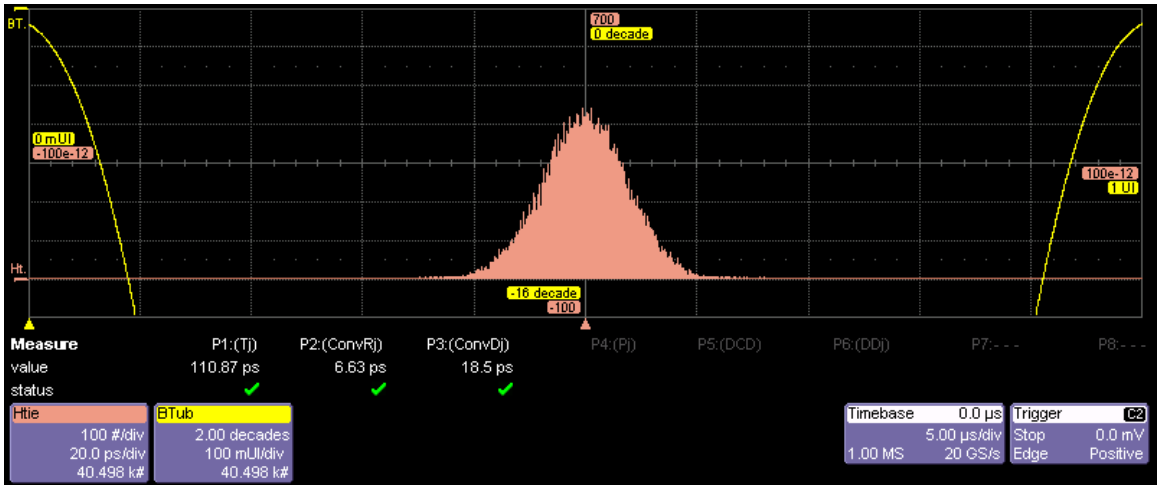
	MOI Reference	Test Criteria
AmpBal max:	TSG-06 - Amplitude Imbalance	within 10%
AmpBal min:	TSG-06 - Amplitude Imbalance	within 10%

- t20-80TX, R/F bal; MFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
t2080 + rise:	Not in IL Test Report	67 ps to 273 ps
t2080 + fall:	Not in IL Test Report	67 ps to 273 ps
t2080 - rise:	Not in IL Test Report	67 ps to 273 ps
t2080 - fall:	Not in IL Test Report	67 ps to 273 ps
t2080 differential Rise:	TSG-02 - Rise/Fall Time	67 ps to 273 ps
t2080 differential Fall:	TSG-02 - Rise/Fall Time	67 ps to 273 ps

Gen 1x Jitter Tests

Example: Edge to Reference Jitter with PLL -3 dB at fbaud/1667 = 0.9 MHz, Damping factor = 0.8, (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)



	limit
TJ:	366.667 ps
DJ:	233.333 ps

Gen 2 Tests

- Amplitude balance, HFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
AmpBal max:	TSG-06 - Amplitude Imbalance	within 10%
AmpBal min:	TSG-06 - Amplitude Imbalance	within 10%

- Tui, ftol, fssc (if SSC); HFTP (6.2.1 Table 2 - General Specifications)

	MOI Reference	Test Criteria
Tui min:	PHY-01 - Unit Interval	>/= 333.2167 ps
Tui max:	PHY-01 - Unit Interval	</= 335.1167 ps
ftol:	PHY-02 – Frequency Long Term Stability	3 GHz ±1.05 MHz
fssc:	PHY-03 - Spread-Spectrum Modulation Frequency	

- t20-80TX, R/F bal; HFTP (6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
t2080 + rise:	Not in IL Test Report	67 ps to 136 ps
t2080 + fall:	Not in IL Test Report	67 ps to 136 ps
t2080 - rise:	Not in IL Test Report	67 ps to 136 ps
t2080 - fall:	Not in IL Test Report	67 ps to 136 ps
Rise Imbalance:	TSG-05 - Rise/Fall Imbalance	< 20%
Fall Imbalance:	TSG-05 - Rise/Fall Imbalance	< 20%
t2080 differential Rise:	Not in IL Test Report	67 ps to 136 ps
t2080 differential Fall:	Not in IL Test Report	67 ps to 136 ps

- **Vdiff min, max tests** (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
DH (Vdiff min HFTP):	TSG-01- Differential Output Voltage	> 400 mV
DM (Vdiff min MFTP):	TSG-01- Differential Output Voltage	> 400 mV
VtestLBP (Vdiff min LBP):	TSG-01- Differential Output Voltage	> 400 mV
pu (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pl (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pu (Vdiff max LFTP):	TSG-01- Differential Output Voltage	
pl (Vdiff max LFTP):	TSG-01- Differential Output Voltage	

- Amplitude balance and Vcm-ac, MFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
AmpBal max:	TSG-06 - Amplitude Imbalance	within 10%
AmpBal min:	TSG-06 - Amplitude Imbalance	within 10%
Vcm,acTX max:	TSG-04 - AC Common Mode Voltage	< 50mV

- t20-80TX, R/F bal; MFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
t2080 + rise:	Not in IL Test Report	67 ps to 136 ps
t2080 + fall:	Not in IL Test Report	67 ps to 136 ps
t2080 - rise:	Not in IL Test Report	67 ps to 136 ps
t2080 - fall:	Not in IL Test Report	67 ps to 136 ps
Rise Imbalance:	TSG-05 - Rise/Fall Imbalance	< 20%
Fall Imbalance:	TSG-05 - Rise/Fall Imbalance	< 20%

t2080 differential Rise:	Not in IL Test Report	67 ps to 136 ps
t2080 differential Fall:	Not in IL Test Report	67 ps to 136 ps

Gen 2i/2m Jitter Tests

- Jitter with PLL -3 dB at fbaud/10 = 300 MHz (Ref #6.2.1 Table 4 - Transmitted Signal Requirements), Damping factor = 0.8

		Test Criteria
TJ:	Not in IL Test Report	< 100.000 ps
DJ:	Not in IL Test Report	

- Jitter with PLL -3 dB at fbaud/500 = 6 MHz (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements), Damping factor = 0.8

	MOI Reference	Test Criteria
TJ:	TSG-11 - TJ at Connector, Clock, 500	</=123.333 ps
DJ:	TSG-12 - DJ at Connector, Clock, 500	</=63.333 ps

Gen2m Tests

- Amplitude balance, HFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
AmpBal max:	TSG-06 - Amplitude Imbalance	within 10%
AmpBal min:	TSG-06 - Amplitude Imbalance	within 10%

- Tui, ftol, fssc (if SSC present); HFTP (Ref # 6.2.1 Table 2 - General Specifications)

	MOI Reference	Test Criteria
Tui min:	PHY-01 - Unit Interval	>/= 333.2167 ps
Tui max:	PHY-01 - Unit Interval	</= 335.1167 ps
ftol:	PHY-02 – Frequency Long Term Stability	3 GHz ±1.05 MHz
fssc:	PHY-03 - Spread-Spectrum Modulation Frequency	

- t20-80TX, R/F bal; HFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
t2080 + rise:	Not in IL Test Report	67 ps to 136 ps
t2080 + fall:	Not in IL Test Report	67 ps to 136 ps
t2080 - rise:	Not in IL Test Report	67 ps to 136 ps
t2080 - fall:	Not in IL Test Report	67 ps to 136 ps
Rise Imbalance:	TSG-05 - Rise/Fall Imbalance	< 20%
Fall Imbalance:	TSG-05 - Rise/Fall Imbalance	< 20%
t2080 differential Rise:	Not in IL Test Report	67 ps to 136 ps
t2080 differential Fall:	Not in IL Test Report	67 ps to 136 ps

- Vdiff min, max tests (Ref #6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
DH (Vdiff min HFTP):	TSG-01- Differential Output Voltage	> 500 mV
DM (Vdiff min MFTP):	TSG-01- Differential Output Voltage	> 500 mV
VtestLBP (Vdiff min LBP):	TSG-01- Differential Output Voltage	> 500 mV
pu (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pl (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pu (Vdiff max LFTP):	TSG-01- Differential Output Voltage	
pl (Vdiff max LFTP):	TSG-01- Differential Output Voltage	

- Amplitude balance and Vcm-ac, MFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
AmpBal max:	TSG-06 - Amplitude Imbalance	within 10%
AmpBal min:	TSG-06 - Amplitude Imbalance	within 10%
Vcm,acTX max:	TSG-04 - AC Common Mode Voltage	< 50 mV

- t20-80TX, R/F bal; MFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
t2080 + rise:	Not in IL Test Report	67 ps to 136 ps
t2080 + fall:	Not in IL Test Report	67 ps to 136 ps
t2080 - rise:	Not in IL Test Report	67 ps to 136 ps
t2080 - fall:	Not in IL Test Report	67 ps to 136 ps
Rise Imbalance:	TSG-05 - Rise/Fall Imbalance	< 20%
Fall Imbalance:	TSG-05 - Rise/Fall Imbalance	< 20%
t2080 differential Rise:	Not in IL Test Report	67 ps to 136 ps
t2080 differential Fall:	Not in IL Test Report	67 ps to 136 ps

Gen2x Tests

Amplitude balance, HFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
AmpBal max:	TSG-06 - Amplitude Imbalance	within 10%
AmpBal min:	TSG-06 - Amplitude Imbalance	within 10%

Tui, ftol, fssc (if SSC); HFTP (Ref # 6.2.1 Table 2 - General Specifications)

	MOI Reference	Test Criteria
Tui min:	PHY-01 - Unit Interval	>/= 333.2167ps
Tui max:	PHY-01 - Unit Interval	</= 335.1167ps
ftol:	PHY-02 – Frequency Long Term Stability	3 GHz ±1.05 MHz
fssc:	PHY-03 - Spread-Spectrum Modulation Frequency	

- t20-80TX, R/F bal; HFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
t2080 + rise:	Not in IL Test Report	67 ps to 136 ps
t2080 + fall:	Not in IL Test Report	67 ps to 136 ps
t2080 - rise:	Not in IL Test Report	67 ps to 136 ps
t2080 - fall:	Not in IL Test Report	67 ps to 136 ps
t2080 differential Rise:	Not in IL Test Report	67 ps to 136 ps
t2080 differential Fall:	Not in IL Test Report	67 ps to 136 ps

- Vdiff min, max tests (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
DH (Vdiff min HFTP):	TSG-01- Differential Output Voltage	> 800 mV
DM (Vdiff min MFTP):	TSG-01- Differential Output Voltage	> 800 mV
VtestLBP (Vdiff min LBP):	TSG-01- Differential Output Voltage	> 800 mV
pu (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pl (Vdiff max MFTP):	TSG-01- Differential Output Voltage	< 0.05
pu (Vdiff max LFTP):	TSG-01- Differential Output Voltage	
pl (Vdiff max LFTP):	TSG-01- Differential Output Voltage	

- Amplitude balance and Vcm-ac, MFTP (Ref #6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
AmpBal max:	TSG-06 - Amplitude Imbalance	within 10%
AmpBal min:	TSG-06 - Amplitude Imbalance	within 10%

- t20-80TX, R/F bal; MFTP (Ref # 6.2.1 Table 4 - Transmitted Signal Requirements)

	MOI Reference	Test Criteria
t2080 + rise:	Not in IL Test Report	67 ps to 136 ps
t2080 + fall:	Not in IL Test Report	67 ps to 136 ps
t2080 - rise:	Not in IL Test Report	67 ps to 136 ps
t2080 - fall:	Not in IL Test Report	67 ps to 136 ps
t2080 differential Rise:	Not in IL Test Report	67 ps to 136 ps
t2080 differential Fall:	Not in IL Test Report	67 ps to 136 ps

THEORY OF OPERATION

This section is based on sections 6.2 and 6.4 of the **Serial ATA II: Electrical Specification**, Revision 1.0, dated 26 May 2004. Section 6.2.1, tables 2 through 7, state the electrical specifications that a SATA host or device must comply with. Below, for most of the items for which a scope can be useful, we will reproduce the table entry with relevant parts of the "detail," "measurement" cross-referenced sections immediately below that, and then we state whether our scripts automate this measurement. If the scripts do not automate it because it is easily measured manually on a LeCroy SDA we will explain how to measure it manually.

Section 6.2.1 Table 2, General specifications

- **Channel Speed and Fbaud** - both nominal, no limits or measurement specified. Channel speed is 1.5 Gb/s for all Gen1 usage models, 3.0 Gb/s for all Gen2 usage models. Fbaud is 1.5 GHz and 3.0 GHz for Gen1 and Gen2, respectively.
- **Frame Error Rate**

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
FER, Frame Error Rate		Max	8.2e-8 at 95% confidence level			8.2e-8 at 95% confidence level			6.2.2.1.2	6.4.1

Because it uses link and transport layers, this measurement cannot be made by a scope. However, this can be measured with a protocol analyzer such as the SAS Tracer or SA Tracer from LeCroy. Both record Protocol errors, including Link level (CRC, RD, R_ERR primitive, etc.), Transport level (Framing error, invalid frame type, etc.), and some Application layer errors (Incomplete ATA commands). Section 6.2.2.1.2 (see below) says frame error detection is based on CRC error detection; statistics on CRC errors can be derived.

6.2.2.1.2 Frame Error Rate

Frame error rate is the measure of link performance using all the intermediate circuit blocks in the chain from low-level Phy Layer, Link Layer, through Transport Layer. Frame error rate is a system level test, not a compliance test. Error detection is at the frame level using the cyclic redundancy check (CRC) error detection mechanism, and respective reporting to the higher layer levels.

6.4.1 Frame Error Rate Testing

Serial ATA error detection at the frame level uses the cyclic redundancy check (CRC) error detection mechanism, and respective reporting to the higher layer levels. Since all frames include a header and CRC field, the calculation includes these overhead bytes in the Frame Error specification.

- **T_{UI}**

T_{UI}, Unit Interval	ps	Min	666.4333	333.2167	6.2.2.1.3	6.4.11
		Nom	666.6667	333.3333		
		Max	670.2333	335.1167		

6.2.2.1.3 Unit Interval

The operating data period (nominal value architecture specific), this value includes the long-term frequency accuracy and the Spread Spectrum Clock FM frequency deviation (rounded to 4 places). This is the time interval value of each cycle of the Reference Clock.

Note: the last sentence of 6.2.2.1.3 was added after the first 1.0 release candidate of the spec. It clarifies the intent of the measurement.

The important thing is not to mix jitter measurement into T_{UI}. Note that the details section mentions only "long term" and SSC. We automate this measurement by forming an "SSC track" and measuring its min and max. The SSC Track is formed by FM demodulation with a bandwidth limit that attenuates jitter similarly to a PLL.

- f_{tol}

f_{tol}, TX Frequency Long Term Stability	ppm	Min	-350	6.2.2.1.4	6.4.6
		Max	+350		

6.2.2.1.4 TX Frequency Long Term Stability

This specifies the allowed frequency variation from nominal; it does not include frequency variation due to jitter, Spread Spectrum Clocking, or phase noise of the clock source.

6.4.6 says, in part:

> "There are several considerations for choosing instruments to measure long term frequency accuracy. The long-term frequency accuracy of the instrument timebase needs to be significantly better than the 350 ppm limit in this specification; many oscilloscopes do not have this frequency accuracy. In general, equivalent-time oscilloscopes cannot be used for this purpose since they require a trigger synchronous with the data.
>
> A method to measure the long-term frequency accuracy is to use a frequency counter. Many spectrum analyzers have frequency counters built in. The test setup in Figure 56 below shows the connections.
>
> The transmitter under test sends a HFTP (D10.2) signal to the spectrum analyzer. The signal may or may not have SSC, a 30 kHz frequency modulation, on it. Set the spectrum analyzer for a center frequency of 750 MHz at Gen1 or 1.5 GHz at Gen2, a frequency span of 100 kHz (with SSC on, frequency span of 20 MHz, resolution BW to 300 kHz, video BW to 300 kHz), a counter resolution of 10 Hz or better (350 ppm at 1.5 GHz is 525 kHz). Then place the marker on the peak signal (center of peaks with SSC on). The counter reads the long-term frequency of the transmitter; the accuracy is a percentage.
>
> When SSC is present, the measurement is a combination of the long-term frequency accuracy and a frequency offset due to the SSC modulation."

Figure 56 of the standard is a diagram showing how to hook up one side of a differential SATA signal to a frequency counter.

We do automate this measurement. The LeCroy SDA's timebase is much better than 350 ppm; its timebase spec is "Clock Accuracy ≤ 1 ppm @ 0-40 °C". To make this measurement the SDA acquires a long enough record so that the effect of SSC is only seen as an offset. It acquires 500 µs which is 10 MS at 20 GS/s. The SDA's Bit Rate parameter computes the required answer. Because the expected answer is different with and without SSC, the scripts ask the user whether SSC is in use.

For very long-term stability a user could manually set up the Bit Rate parameter on a 500 µs (10 MS at 20 GS/s) acquisition, and create a Trend of BitRate values. The Trend accumulates one Bit Rate result per sweep. A long enough Trend could show long-term frequency variation over hours.

- f_{ssc}

f_{ssc}, Spread-Spectrum Modulation Frequency	kHz	Min	30	30	6.2.2.1.5 6.3.3	6.4.11
		Max	33	33		

6.2.2.1.5 says, in its entirety,

> "The modulation frequency of the Spread-Spectrum frequency modulation. See further details of Spread-Spectrum in Section 6.3.3."

6.3.3 describes SSC.

6.4.11 says, in part:

> "Spread Spectrum Clocking is intentional low frequency modulation of the bit clock. The SSC profile is the modulation on the bit clock. To measure the SSC profile, a frequency demodulator and low pass filter are necessary. There are many possible realizations of this, in hardware and software. The low pass filter is

necessary to reject undesired post-demodulation frequency components from bit patterns and jitter. To minimize these undesired signals the HFTP bit pattern shall be used. This can be produced using the BIST FIS to invoke the Transmit-Only option. The SSC Profile measurement is also used to determine the Unit Interval values.

A single-shot capture oscilloscope can be used to measure the times of zero crossings (through interpolation) and perform the FM demodulator and low pass filter function. The memory record of the oscilloscope must be long enough to achieve the low pass filter cutoff frequency. The long term frequency accuracy of the oscilloscope time base should be significantly better than the 350 ppm limit in this specification."

This addresses the SDA perfectly. We automate this measurement. If the user specifies that SSC is in use, the scripts put up a parameter to measure the frequency of the SSC Track. The SSC Track is described in the measurement of T_{UI}, above. If the user says SSC is not in use this measurement is not made.

- **SSC_{tol}**

SSC_{tol}, Spread-Spectrum Modulation Deviation	ppm	Min	-5000	-5000	6.2.2.1.6 6.3.3	6.4.11
		Max	+0	+0		

6.2.2.1.6 Spread-Spectrum Modulation Deviation

This is the allowed frequency variation from nominal due to the SSC AC modulation expressed in terms of the unit interval deviation from the unit interval value of the long-term frequency value. See further details of Spread Spectrum in Section 6.3.3.

Relevant parts of 6.4.11 were excerpted above for f_{SSC}.

Our scripts do not produce a separate value for this. They do automate the measurement of T_{UI}, which has limits 350 ppm shorter and 5350 ppm longer than nominal. Those limits are the sum of the limits of SSC_{tol} plus the limits of ftol. The signal the SDA sees includes the ftol of +/- 350 ppm allowed as well as the modulation due to SSC, so if the signal passes T_{UI}, then the modulation deviation almost certainly passes SSC_{tol}; if the signal passes T_{UI} with more than 350 ppm to spare on each side, then the modulation deviation definitely passes SSC. The limits on SSC_{tol} are, in fact, limits, not goals; in all circumstances they cannot be exceeded. Therefore it is likely that a signal from a SATA host or device in a nice environment will pass T_{UI} with more than 350 ppm to spare on each side.

- **$V_{cm,dc}$**

$V_{cm,dc}$, DC Coupled Common Mode Voltage	mV	Min	200	-	-	6.2.2.1.7	6.4.4
		Nom	250	-	-		
		Max	450	-			

Only specified for Gen1i and Gen1m in the table. Gen1x and Gen2 are AC coupled, as stated in 6.2.2.1.7.

"6.2.2.1.7 DC Coupled Common Mode Voltage (Gen1i)

The Common mode DC level is defined as [(TX+) + (TX-)]/2 and [(RX+) + (RX-)]/2 measured at the mated connector. This requirement only applies to Gen1i DC-coupled designs (no blocking capacitors) that hold the common-mode DC level at the connector. The four possible common mode biasing configurations shown in Figure 13 below demonstrate that only DC-coupled designs need sustain the specified common-mode level to ensure interoperability. AC coupled designs may allow the DC level at the connector to float. The SATA interfaces defined as Gen1x, Gen2i, Gen2x shall be AC-coupled and this requirement does not apply to these.

A DC-coupled receiver shall weakly hold the common-mode level of its inputs to the $V_{cm,dc}$ value specified in Table 2. A DC-coupled transmitter shall transmit with the $V_{cm,dc}$ value specified in Table 2 while driving into a 100 ohm differential impedance."

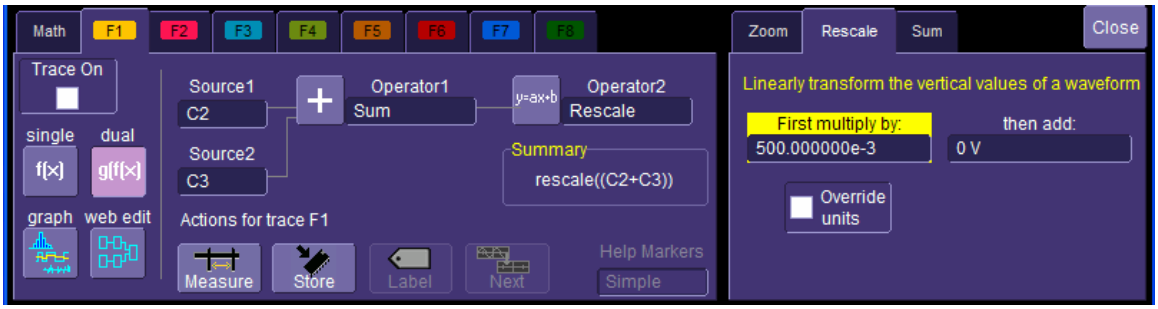
Note that 6.2.2.17 does not refer to Gen1m or Gen2m. Those were added after the first 1.0 release candidate of the specification. This has been addressed by errata and will be corrected in a future release of the specification. In most cases Gen1m is like Gen1i, and Gen2m is like Gen2i, as in this case.

Section 6.4.4 says, in part:

> "The transmit DC offset voltage (for Gen1i only) can be measured with the setup in Figure 52. The HBWS is measuring a DC voltage and the DC blocks must not be present."

HBWS stands for High Bandwidth Scope, defined in the specification as having 10 GHz BW or more and assumed to be a sampling scope. A LeCroy SDA 11000 meets the definition of a HBWS.

We do not automate this measurement. To make this measurement manually, a user could configure a math function to be (C2 + C3) / 2, as shown below:



Then TX+ and TX- and then RX+ and RX- to C2 and C3, and verify that resulting trace does not exceed the limits of Vcm,dc. It is very important that the deskew procedure be performed before making this measurement. Skew between the inputs will cause spikes in the sum of C2+C3 at each transition, in the polarity of the input that is earlier in time.

- **$V_{cm,ac\ coupled}$**

$V_{cm,ac\ coupled}$, **AC Coupled Common Mode Voltage**	mV	Min	0	-	-	6.2.2.1.8	6.4.25
		Max	2000	-	-		

Again, only specified for Gen1i and Gen1m.

Section 6.2.2.1.8 says, in part:

> "The AC coupled common mode voltage in Table 2 defines the open circuit DC voltage level of each single-ended signal at the IC side of the coupling capacitor in an AC coupled PHY and it shall be met during all possible power and electrical conditions of the PHY including power off and power ramping. Since the Gen1x, Gen2i, Gen2x specification defines only the signal characteristics as observable at the connector, this value is not applicable to those specifications."

Again, the reference to Gen2i applies also to Gen2m.

Since this measurement is not made at the SATA connector, it cannot be made using the TF-SATA test fixture; instead, suitable probes at the appropriate points must be used. And since it must be tested during "all possible power and electrical conditions of the PHY" it is beyond the ability of a script controlling a measuring instrument to automate. Therefore our scripts do not automate this measurement.

- **Z_{diff} - differential impedance**

Only specified for Gen1i and Gen1m. Only a nominal value of 100 ohms is given in the table. The "detail" section says, in its entirety:

> ***6.2.2.1.9 Nominal Differential Impedance (Gen1i)***
>
> The Nominal impedance of all components in a SATA system.
>
> The measurement description specifies use of a TDR:

6.4.22 TDR Differential Impedance (Gen1i / Gen1m)

This specification describes transmitter output impedance and receiver input impedance in terms of the peak value of a reflection given an incident step of known risetime.

Since the SATA adapter is not included when setting risetime, good matching and low loss are necessary in the adapter to minimize errors in the measured TDR impedance.

The figure showing the measurement setup shows a differential TDR. The LeCroy SDA does not provide TDR functionality, so the scripts do not automate this or any other impedance measurement. Note, however, that LeCroy's TF-SATA has substantially better matching and lower loss than the reference (Gen1) test fixture, and is appropriate for making this measurement.

- **AC coupling capacitance**

$C_{ac\ coupling}$ AC Coupling Capacitance	nF	Max	12	12	6.2.2.1.10	6.4.14

6.4.14 AC Coupling Capacitor

This measurement is only applicable to AC coupled transmitters and receivers. The AC coupling capacitor value is not directly observable at the SATA connector. In order to measure this capacitance, each signal must be probed on both sides of the AC coupling capacitor. The unit under test is powered off and nothing is plugged into the SATA connector. In the case of coupling within the IC or where there is no access to the signals between the IC and external coupling capacitors, this parameter is not measurable as shown.

The figure shows a "Capacitance Meter" connected to both sides of one of the coupling capacitors. Because this measurement cannot be made at the SATA connector (the "compliance point"), and because the SDA is not a capacitance meter, our scripts do not automate this measurement.

- **common mode transient settling time**

$t_{settle,cm}$, Common Mode Transient Settle Time	ns	Max	10	-	6.2.2.3.6	-

Note that this spec only applies to Gen1i. That is shown in the table and spelled out in 6.2.2.3.6.

Note that no measurement method is defined. A scope such as a LeCroy SDA is a good tool to make this measurement.

Our scripts do not automate this measurement.

To perform this measurement manually, the only difficulty is capturing a common mode transient. If it is required to trigger on a common mode transient a means to sum the two differential signals to produce Vcm (actually, 2*Vcm) external to the scope must be provided so that the common mode signal can be supplied to the scope. If that is done a simple edge trigger will catch transients. If the scope can be triggered on some other signal that coincides with a common mode transient, the external hardware is not needed; the scope can create the common mode signal by summing the differential inputs (and dividing by 2), as shown in the picture of the F1 setup dialog above in the section on Vcm,dc.

- **Vtrans**

V_{trans}, Sequencing Transient Voltage	V	Min	-2.0	-2.0	6.2.2.1.11	6.4.13
		Max	2.0	2.0		

6.2.2.1.11 says, in part:

> "This parameter addresses the transient voltages on the serial data bus during power sequencing and power mode changes . . . This measurement shall include the test conditions of power on and power off ramping at the fastest possible rate expected in systems using the PHY, as well as any power mode transitions."

6.4.13 Sequencing Transient Voltage

Figure 70 shows the connections to the receiver or transmitter under test. Each RX or TX line is terminated to ground with a minimum impedance of 10 M Ohm that includes the probe and any external load. The value of the voltage transients during power on or power off sequencing, or power state changes seen at Vp or Vn, shall remain in the voltage range specified.

Figure 70 shows both sides of the differential signal from the SATA adapter (ie, LeCroy's TF-SATA) going through 50 ohm cables to 10Mohm terminations. It does not specify what device measures Vp and Vn. The SDA as supplied cannot make this measurement because of the 10M ohm requirement.

That concludes the items in Table 2.

Section 6.2.1 Table 3, Transmitter Specifications:

All items in this table are impedances and return loss measurements. Since the SDA does not provide TDR or VNA functionality, our scripts do not automate any of these measurements. Please see the current Serial ATA II: Electrical Specification for more information about these measurements.

Section 6.2.1 Table 4, Transmitted Signal Requirements:

Our scripts automate most of the measurements in this table.

- **Vdiff Tx**

V_{diffTX}, TX Differential Output Voltage	mVppd	Min	400	800	400	800	6.2.2.3.1	6.4.4
		Nom	500	-				
		Max	600	1600	700	1600		

The method for making this measurement is quite complex, based on statistics, and our scripts do automate these measurements. The measurement method changed from that in the first release candidate of the spec.

6.2.2.3.1 says, in part:

> ". . .This is measured at mated Serial ATA connector on transmit side including any pre-emphasis."

6.4.4 Transmitter Amplitude

The transmitter amplitude values are specified in Table 4:

> "Transmitted Signal Requirements refer to the output signal from the unit under test (UUT) at the mated connector into a Laboratory Load (LL) (for Gen1i, Gen2i, Gen1x, and Gen2x), or from the unit under test through a Compliance Interconnect Channel (CIC) into a Laboratory Load (for Gen1x and Gen2x only). The signals are not specified when attached to a system cable or backplane.
>
> Transmitter amplitude is measured with each of three waveforms: HFTP, LFTP, and the Lone bit pattern. Amplitude specifications shall be met during each bit within the specified patterns. For example, the "lone-bit" within the Lone Bit Pattern is often of lower amplitude than most bits.
>
> The minimum amplitude value is measured 0.5UI after a Reference Clock edge (defined in section 6.3.2). The Reference Clock defines the ideal (zero jitter) zero crossing times. The maximum amplitude is measured across the entire waveform. . .
>
> Figure 52 and Figure 53 show test setups for measuring transmitter amplitude. The HBWS is the standard for measuring amplitude. The losses in the test connections can be significant so it is prudent to minimize and estimate these. Our scripts automate these tests."

Figures 52 and 53 (and Figure 48 in section 6.4.2) show either a HBWS (High Bandwidth Scope, defined as 10 GHz BW or more and assumed to be a sampling scope) or a JMD, a Jitter Measuring Device. A LeCroy SDA 11000 meets the definition of a HBWS. A LeCroy SDA 6 GHz BW scope qualifies as a JMD, which allows an SDA 6000A or SDA 6020 to make these measurements. However, that is not the intent of the spec. Because a 5th harmonic of a 3 Gb/s signal is above the bandwidth of a 6 GHz scope, it is possible that the shape it shows will be affected by missing the 5th harmonic. (Note: 7th harmonic is above 10 GHz.) Since the absence of 5th harmonic should make a square pulse higher near the edges, and lower in the middle, using a 6 GHz scope should use up margin on both Vdiff max (measured over an entire UI) and Vdiff min (measured only around the middle of a UI).

That means it should be harder to pass: if your signal does pass Vdiff tests on a 6 GHz SDA it will probably pass on a HBWS. If it does not pass on a 6 GHz SDA it just might pass on a SDA 11000 or other HBWS. Therefore we print the following disclaimer about Vdiff measurements in our reports:

> Note: According to the spec, these tests require 10 GHz of bandwidth. If this test is performed with 6 GHz bandwidth, it should be harder to pass due to absence of the 5th harmonic. Even so, results with 6 GHz of bandwidth must be regarded as an indicator and not the true compliance test.

Section **6.4.2 Measurement of Differential Voltage Amplitudes** defines the measurement methodology for Vdiff min and max test. Interestingly, there are no explicit references to section 6.4.2 from other sections of the **Serial ATA II: Electrical Specification** Revision 1.0. However, this is the section that defines the complex measurement methodology for these tests. This has been addressed by errata and will be corrected in a future release of the specification. This section is eleven pages long in the spec, please see the current version of the **Serial ATA II: Electrical Specification** for details of the measurement method.

Please see the **Serial ATA II: Electrical Specification** section **6.2.7 Compliance Interconnect Channels (Gen1x, Gen2x)** for definition of the CIC for Gen1x and Gen2x. The CIC is also used in jitter measurements for Gen1x and Gen2x.

LeCroy's TF-SATA has been evaluated by an independent laboratory and can serve as part of a Laboratory Load. The cables supplied with TF-SATA are Semflex SW-180 30-inch cables with SMA connectors. More information about the cables can be found at www.semflex.com, a datasheet for the SW line is at http://www.semflex.com/pdf/SW%20Series.pdf. Any high quality, fairly short cables, approximately matched in length, can be used. Remember to perform the deskew procedure.

The LeCroy SDA has been tested and found to qualify as a laboratory load.

- **Measurement interval for VdiffTX,min**

UI_{VminRX}, TX Minimum Voltage Measurement Interval	UI		-	0.5	0.45-0.55	0.5	6.2.2.3.2	6.4.4

Clearly, the abbreviation shown above from Table 4 should say UI_{VminTX} ; UI_{VminRX} is redefined differently in Table 6 for Receiver Tolerance Testing. This is just a specification used in performing the measurement of VdiffTX,min. The "detail" section, in its entirety, is:

> ***6.2.2.3.2 TX Minimum Voltage Measurement Interval***
>
> The point within a UI where the signal shall meet minimum levels. An excerpt from section 6.4.4 appears above, under VdiffTX.

- **$t_{20\text{-}80TX}$**

$t_{20\text{-}80TX}$, TX Rise/Fall Time	ps (UI)	Min 20-80%	100 (.15)	67 (.10)	67 (.20)	6.2.2.3.3	6.4.3
		Max 20-80%	273 (.41)	273 (.41)	136 (.41)		

6.2.2.3.3 TX Rise/Fall Time

Rise times and fall times are measured between 20% and 80% of the signal, see Figure 18. The Rise and fall time requirement $t_{r/f}$ applies to differential transitions (TX+ - TX-), for both In-Band and Out-Of-Band signaling.

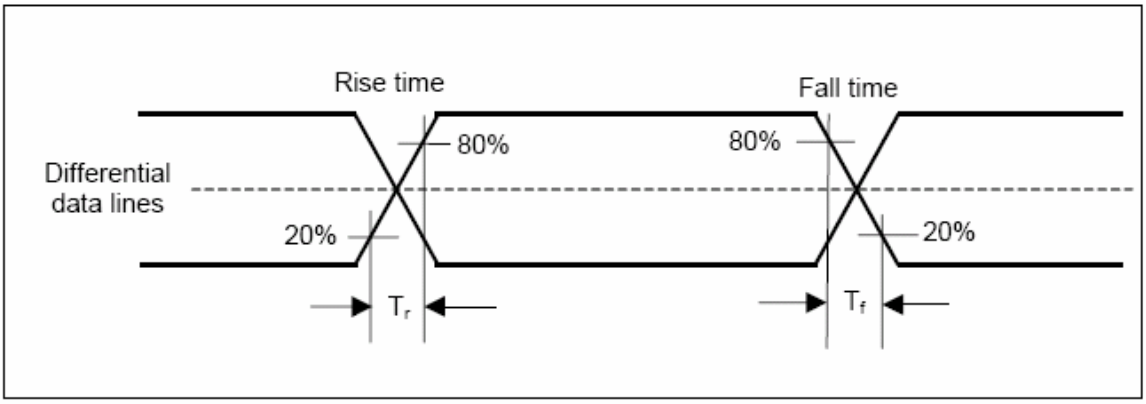


Figure 18: Signal rise and fall times

The above text is clear, however Figure 18 shows a measurement being made on one side of the differential signal. The measurement methodology in 6.4.3 does not help:

6.4.3 says:

> "6.4.3 Rise and Fall Times
>
> The rise and fall times of the waveform under test are defined over a 20%-80% output level change from the High and Low reference levels. High Reference level of the waveform under test is the "mode" of the top portion while the Low Reference level is the "mode" of the bottom portion. Mode is measured using Statistical Methods of the desired waveform and is the most common value of the probability density function.
>
> Therefore, Rise Time = X2 - X1; where X2 is the mean horizontal time value corresponding to 80% of the distance between the Low and High value and X1 is the mean horizontal time value position corresponding to 20% of the distance between the Low and High value.
>
> And Fall Time = X1 - X2; where X1 is the mean horizontal time value corresponding to 20% of the distance between the Low and High value and X2 is the mean horizontal time value position corresponding to 80% of the distance between the Low and High value.

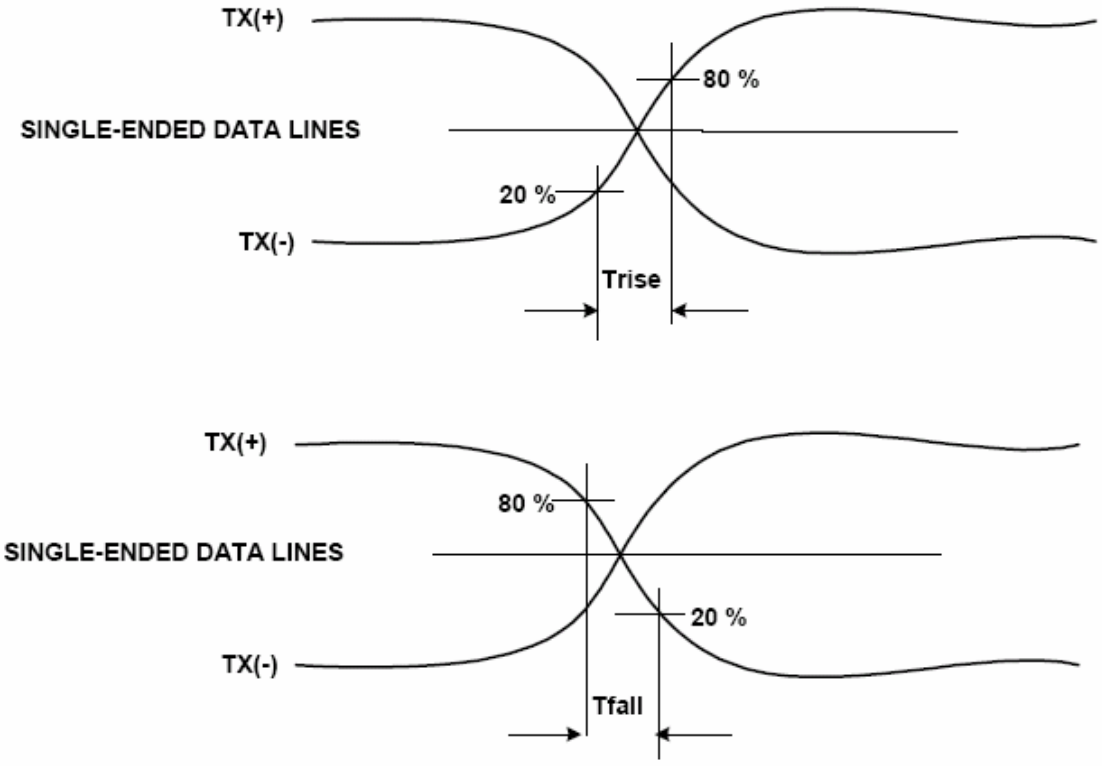


Figure 51: Single Ended Rise and Fall Time

Rise and Fall values are measured using the HFTP, LFTP, and Lone Bit Patterns previously defined.

The rise and fall times for transmitter differential buffer lines are measured with the load fixture shown in Figure 52. The rise and fall times shall be measured with an HBWS.

Note that Figure 51 shows single ended rise and fall times, and the text of this section appears to describe that, which appears to be at odds with the phrase from 6.2.2.3.3: “Rise and fall time requirement $t_{r/f}$ applies to differential transitions (TX+ - TX-)”.

Our scripts measure both the differential rise and fall times (on TX+ - TX-) and the one-side rise and fall times. The text of the 6.2.2.3.3 controls; only the differential rise and fall times are required to pass. It should be expected that rise and fall times on each side are well matched. Below we will see that there is a specification for how well they must match, which applies to Gen2i and Gen2m only. The four one-side rise and fall times are reported for your information; they are not individually required to pass these limits.

Figure 52 shows either a HBWS or a JMD. A 6 GHz SDA is capable of measuring transition times below 67ps with good accuracy. The text of the spec states that these measurements “shall” be made with a HBWS. An SDA 11000 is a HBWS. The SDA 6000A’s or SDA 6020’s readings should substantially agree with those of a HBWS. A disclaimer is not printed in our report about this.

- **TskewTX**

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
t_{skewTX}, TX Differential Skew	ps	Max	20			20		15	6.2.2.3.4	6.4.12

6.2.2.3.4 says, in part:

> "6.2.2.3.4 TX Differential Skew (Gen2i, Gen1x, Gen2x)
>
> TX Differential Skew is the time difference between the single-ended mid-point of the TX+ signal rising/falling edge, and the single-ended mid-point of the TX- signal falling/rising edge. . ."

The measurement section, 6.4.12, says in part:

> "6.4.12 Intra-pair Skew
>
> Intra-pair skew measurements are important measurements of transmitters and receivers . . . As the measurement values are typically just a few picoseconds, care must be taken to minimize measurement error. Figure 66 illustrates a test setup for a measurement method using a HBWS and its built-in processing. . . Use HFTP and MFTP as the test patterns when measuring transmitter skew."

It is important to perform the deskew procedure (to remove skew due to the cables and difference between SDA channels) before making this measurement. Although the required deskew setting should be quite small, even a couple of ps saved can make a difference as it is a significant part of the limit for this measurement.

Section 6.4.12 describes a way of measuring this with a HBWS, specifically a sampling scope. It requires DC blocks at the HBWS's inputs. It uses TX+ and the inversion of TX+ to make a crossing; and TX- and the inversion of TX- to make another crossing; the time between those crossings is the TX differential skew. This measurement method guarantees that both crossings will be at 50%.

Section 6.4.12 does not mandate use of a HBWS, but only "illustrates . . . a measurement method" using an HBWS.

Our scripts do not automate this measurement, partly because it is very easy to set up manually. Set up P1 to be "Skew" (found in the Horizontal parameter group) of C2 to C3. Be sure to set Slope to "Both" on both the Skew Clock 1 and Skew Clock 2 tabs on the right-hand dialog. The default settings tell it to measure at 50% level; that is good. Statistics should be on; if they are not select **Statistics On** from the **Measure** drop-down menu. The measurement result is the **mean** of P1.

Note that since the **mean** averages together skew values when T+ rises (and T- falls) with skew values when T- rises (and T+ falls), any small inaccuracy in the 50% level computation is not critical. For example, if the level is slightly low, T+ rising through the level will be earlier than T- falling through the level. But when T- rises and T+ falls the level cross of T+ will be later than T- by the same amount of time. That is exactly true if T+ and T- have the same rise times and both have the same fall times. Rise and fall times can differ, that does not affect the cancellation. Since there must be an equal number of rising and falling transitions observed (actually, +/- 1 but with a long enough acquisition that becomes insignificant to the mean), skew introduced by level error does not affect the **mean**.

- **Vcm,acTX**

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
$V_{cm,acTX}$, TX AC Common Mode Voltage	mVp-p	Max	-			50		-	6.2.2.3.5	6.4.17

6.2.2.3.5 TX AC Common Mode Voltage (Gen2i, Gen1x, Gen2x)

Maximum sinusoidal amplitude of common mode signal measured at the transmitter connector.

The Transmitter shall comply to the electrical specifications of section 6.2, when subjected to a sinusoidal interfering signal with peak-to-peak voltage, and swept from the frequency range extremes, at a sweep rate period no shorter than 33.33 µs.

6.4.17 TX AC Common Mode Voltage

This parameter is a measure of common mode noise other than the CM spikes during transitions due to TX+/TX- mismatch and skews which are limited by the rise/fall mismatch and other requirements. Measurement of this parameter is achieved by transmitting through a mated connector into a Lab Load as shown in Figure 52. The transmitter shall use an MFTP (mid-frequency test pattern). The measurement instrument may be a HBWS or other instrument with analog bandwidth of at least 3 * bitrate / 2.

Separate channels must be used for TX+ and TX- and the common mode is (TX+ + TX-) / 2. This raw common mode shall be filtered with a first order filter having a cutoff equal to the bitrate / 2 to remove the noise contribution from the edge mismatches. The peak-to-peak voltage of the filter output is the AC Common Mode Voltage and shall remain below the specified limit.

For reference, Figure 52 is reproduced below:

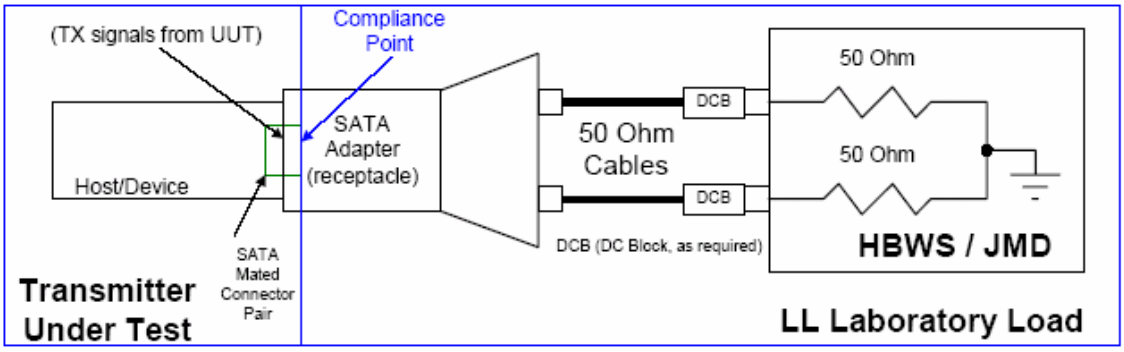


Figure 52: Transmit Amplitude Test with Laboratory Load

Note that 6.2.2.3.5 specifies that it applies to usage models Gen1x and Gen2x, which conflicts with the Table entry. It specifies adding a sine wave, while the measurement methodology in 6.4.17 says it is measuring common mode noise, specifies direct connection to a scope, and refers to a figure showing those connections; it does not use an added sine wave. (The added sine wave is used in receiver tolerance testing.)

We automate this test for the usage models specified in Table 4, measured using the method specified the Measurement section, 6.4.17.

- **$D_{VdiffOOB}$**

$D_{VdiffOOB}$, OOB Differential Delta	mV	Max	-	25	25	6.2.2.3.7	6.4.19

6.2.2.3.7 says, in part:

> 6.2.2.3.7 OOB Differential Delta (Gen2i, Gen1x, Gen2x)
>
> The difference between the average differential value during the idle bus condition and the average differential value during burst on transitions to and from the idle bus condition. . .”

6.4.19 says:

> **6.4.19 OOB Differential Delta**
>
> This parameter is a measure of the offset between the differential voltage of idle times during OOB generation and the average differential voltage during the OOB bursts. The test setup shown in Figure 52 shall be used for this measurement. A HBWS or single-shot scope may be used for this measurement, the DUT shall be configured to send an OOB sequence or multiple OOB sequences, and the instrument shall be configured so that at least 40 Gen 1 UI worth of idle time before the first OOB burst in a sequence and at least 40 Gen 1 UI worth of burst activity in the first OOB burst of a sequence are observed.
>
> The differential signal is TX+ - TX- and the differential voltage during idle for this parameter is determined by averaging the differential voltage of a 40 Gen1 UI span of idle time within the last 60 Gen1 UIs worth of time prior to the first OOB burst in a sequence. The average differential voltage during active time for this parameter is determined by averaging the differential voltage of a 40 Gen1 UI span of time within the first 60 Gen1 UIs of the first burst in a sequence. The use of a span of 40 Gen1 UIs ensures that no matter what the starting time within the burst, the signal will be DC balanced and the average will represent the differential mean. The reason that the active span is taken within the first 60 Gen1 UIs of the first burst in a sequence is to minimize the affect of AC coupling RC time constant on the resulting differential offset if one exists.”

Our scripts to not automate OOB tests. $D_{VdiffOOB}$ is easy to measure manually. Use the Mean parameter (found in the Vertical group) and use the measure gate to isolate the measured regions on TX+ and TX- as required by 6.4.19.

- **D_{VcmOOB}, OOB Common Mode Delta**

D_{VcmOOB}, OOB Common Mode Delta	mV	Max	-	50	50	6.2.2.3.8	6.4.18

6.2.2.3.8 says:

> **"6.2.2.3.8 OOB Common Mode Delta (Gen2i, Gen1x, Gen2x)**
>
> The difference between the common mode value during the idle bus condition and the common mode value during a burst on transitions to and from the idle bus condition."

6.4.18 says:

> **"6.4.18 OOB Common Mode Delta**
>
> This parameter is a measure of the offset between the common mode voltage of idle times during OOB generation and the common mode voltage during the OOB bursts. The test setup shown in Figure 52 shall be used for this measurement. A HBWS or single-shot scope may be used for this measurement, the DUT shall be configured to send an OOB sequence or multiple OOB sequences, and the instrument shall be configured so that at least 40 Gen 1 UI worth of idle time before the first OOB burst in a sequence and at least 40 Gen 1 UI worth of burst activity in the first OOB burst of a sequence are observed.
>
> The common mode signal is (TX+ + TX-)/2 and the common mode voltage during idle for this parameter is determined by averaging the common mode voltage of a 40 Gen1 UI span of idle time within the last 60 Gen1 UIs worth of time prior to the first OOB burst in a sequence. The average common mode voltage during active time for this parameter is determined by averaging the common mode voltage of a 40 Gen1 UI span of time within the first 60 Gen1 UIs of the first burst in a sequence. The reason that the active span is taken within the first 60 Gen1 UIs of the first burst in a sequence is to minimize the affect of AC coupling RC time constant on the resulting common mode offset if one exists."

Our scripts to not automate OOB tests. **D_{VcmOOB}** is easy to measure manually. Use a math function to form the common mode signal, as specified above for Vcm,dc. Use the mean parameter (found in the Vertical group) and use the measure gate to isolate the measured regions of the common mode signal, as required by 6.4.19.

- **TX rise, fall imbalance.**

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
R/F_{bal}, TX Rise/Fall Imbalance	%	Max	-			20		-	6.2.2.3.9	6.4.16

6.2.2.3.9 says:

> "6.2.2.3.9 TX Rise/Fall Imbalance
>
> The match in the rise of TX+ and fall of TX- determined by the functions: absolute value(TX+,rise - TX-,fall)/average where average is (TX+,rise + TX-,fall)/2 and all rise and fall times are 20-80%.
>
> The match in the fall of TX+ and rise of TX- determined by the function: absolute value(TX+,fall - TX-,rise)/average where average is (TX+,fall + TX-,rise)/2 and all rise and fall times are 20-80%."

6.4.16 says:

> "6.4.16 TX Rise/Fall Imbalance
>
> This parameter is a measure of the match in the simultaneous single-ended rise/fall or fall/rise times of the Transmitter. The test setup shown in Figure 52 shall be used for this measurement. This parameter shall be measured and met with both the HFTP and MFTP patterns.
>
> In order to determine the imbalance, the single ended 20-80% rise and fall times of both TX+ and TXshall be determined for a given pattern. Two imbalance values for that pattern are then determined by the two equations:
>
> absolute value(TX+,rise - TX-,fall)/average, where average is (TX+,rise + TX-,fall)/2
>
> absolute value(TX+,fall - TX-,rise)/average, where average is (TX+,fall + TX-,rise)/2
>
> Both values for each pattern shall be less than the maximum listed in Table 4: Transmitted Signal Requirements."

Our scripts automate this measurement.

- **Amplitude imbalance**

Amp_{bal}, TX Amplitude Imbalance	%	Max	-	10	10	6.2.2.3.10	6.4.15

6.2.2.3.10 says:

> "6.2.2.3.10 TX Amplitude Imbalance (Gen2i, Gen1x, Gen2x)
>
> The match in the amplitudes of TX+ and TX- determined by the function: absolute value(TX+ amplitude - TX- amplitude)/average where average is (TX+ amplitude + TX- amplitude)/2 and all amplitudes are determined by mode (most prevalent) voltage."

Again, it is clear from the table that this also applies to Gen2m.

6.4.15 says:

> "6.4.15 TX Amplitude Imbalance
>
> This parameter is a measure of the match in the single-ended amplitudes of the TX+ and TX- signals. The test setup shown Figure 52 shall be used for this measurement. This parameter shall be measured and met with both the HFTP and MFTP patterns. Clock-like patterns are used here to enable the use of standard mode-based amplitude measurements for the sole purpose of determining imbalance. The measurement of differential amplitude uses a different method.
>
> In order to determine the amplitude imbalance, single ended mode high and mode low based amplitudes of both TX+ and TX- over 10 to 20 cycles of the clock-like pattern being used shall be determined. The amplitude imbalance value for that pattern is then determined by the equation:
>
> absolute value(TX+ amplitude - TX- amplitude)/average where average is (TX+ amplitude + TX- amplitude)/2
>
> The amplitude imbalance value for each pattern shall be less than the maximum listed in Table 4: Transmitted Signal Requirements."

Our scripts automate this measurement.

Section 6.4.15 mentions that "measurement of differential amplitude uses a different method". Section 6.4.2 Measurement of Differential Voltage Amplitudes defines the measurement methodology for V_{diff} min and max tests, as mentioned under V_{diffTX}, above.

- **Jitter measurements**

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
TJ at Connector, Data-Data, 5UI	UI	Max	0.355		-	-			6.2.2.3.11 6.3	-
DJ at Connector, Data-Data, 5UI	UI	Max	0.175		-	-				
TJ at Connector, Data-Data, 250UI	UI	Max	0.47		-	-				
DJ at Connector, Data-Data, 250UI	UI	Max	0.22		-	-				
TJ at Connector, Clk-Data, $f_{BAUD}/10$	UI	Max	-			0.30		-	6.2.2.3.12 6.3	6.4.7 6.4.8
DJ at Connector, Clk-Data, $f_{BAUD}/10$	UI	Max	-			0.17		-		
TJ at Connector, Clk-Data, $f_{BAUD}/500$	UI	Max	-			0.37		-		
DJ at Connector, Clk-Data, $f_{BAUD}/500$	UI	Max	-			0.19		-		
TJ after CIC, Clk-Data, $f_{BAUD}/1667$	UI	Max	-		0.55	-		0.55		
DJ after CIC, Clk-Data, $f_{BAUD}/1667$	UI	Max	-		0.35	-		0.35		

6.2.2.3.11 Data-to-Data Transmit Jitter (Gen1i)

The Serial ATA interface jitter characteristics shall comply to within the jitter budget allocations in Table 3. This does not include UI error due to frequency skew (XTAL or SSC related).

Data-to-Data jitter requirements only apply to Gen1i. Data-to-Data jitter is a measure of variance in the zero crossing times of edges at a fixed time (t_n) equal to an integer number of Unit intervals (n) after triggering on data edges (t_0). Since t_0 is triggered from the serial signal rather than a Reference Clock the resulting measurements do represent a combination of the jitter at t_0 and t_n.

6.2.2.3.12 Clock-to-Data Transmit Jitter (Gen2i, Gen1x, Gen2x)

Gen1x, Gen2i, and Gen2x use a Clock-to-Data jitter requirement. Transmitters shall meet the jitter specifications for both tracking PLL frequency corners. Table 4 shows the maximum amount of jitter that a transmitter can generate and still be SATA compliant and section 6.4.8 describes the measurement. Since this specification places the compliance point at the connector, any jitter generated at the package

connection, on the printed circuit board, and at the board connector shall be included in the measurement.

6.3 Jitter

This section defines jitter for SATA II, including Gen2i, Gen2x, and Gen1x. Gen 1i and measurement techniques are explained in SATA 1.0a but are copied here for completeness. . .

Section 6.3 is an excellent description of what jitter is and the different measurement methods required by the Serial ATA ii specification. It is five pages long and is not reproduced here. Please see it in the current Serial ATA II: Electrical Specification.

6.4.7 Jitter Measurements

"This section does not apply to Gen1i jitter measurements.

Jitter is the difference in time between a data transition and the associated Reference Clock event, taken as the ideal point for a transition. The causes of jitter are categorized into random sources (RJ) and deterministic sources (DJ). Although the total jitter (TJ) is the convolution of the probability density functions for all the independent jitter sources, this specification defines the random jitter as Gaussian and the total jitter as the deterministic jitter plus 14 times the random jitter. The TJ specifications of Table 4 and Table 6 were chosen at a targeted BER of 10^{-12}. The BERT scan method described in section 6.4.7.1 is the only method that measures the actual TJ and is used as the reference for all TJ estimation methods. The method for estimating TJ is unique to each measurement instrument. . ."

Section 6.4.7 describes in detail the jitter measurements used for all the new usage models, and is worthwhile reading. We are pleased to be able to refute the assertion that only a BERT scan measures actual TJ; the LeCroy SDA also measures actual TJ and we have verified correlation between its results and a BERT scan.

6.4.8 Transmit Jitter

"The transmit jitter values specified in Table 4 refer to the output signal from the unit under test (UUT) at the mated connector into a Laboratory Load (LL) (for Gen1i, Gen2i, Gen1x, and Gen2x), or from the unit under test through a Compliance Interconnect Channel (CIC) into a Laboratory Load (for Gen1x and Gen2x). The signals are not specified when attached to a system cable or backplane. All the interconnect characteristics of the transmitter, package, printed circuit board traces, and mated connector pair are included in the measured transmitter jitter. Since the SATA adapter is also included as part of the measurement, good matching and low loss in the adapter are desirable to minimize its contributions to the measured transmitter jitter.

Transmit jitter is measured with each of the specified patterns in section 6.2.4.3. The measurement of jitter is described in section 6.4.7. . . ."

Please see the current Serial ATA II: Electrical Specification for the full text of sections 6.4.7 and 6.4.8. The CIC is defined in section 6.2.7 of the specification.

Our scripts automate the jitter tests, both data-to-data (which the SDA calls "edge-edge") and clock-to-data (which the SDA calls "edge-ref"). For clock-to-data measurements, the SDA derives the reference clock using a software PLL that complies with the requirements of **6.3.2 Reference Clock Definition**. The scripts set corner frequencies as required (actually, they set natural frequency which will result in the required -3 dB frequency) and damping factor of 0.8, which is within the allowed range.

LeCroy SDA has been tested and found to qualify as a laboratory load.

The patterns specified in section 6.2.4.3 are too long to be set up using a BIST Activate FIS (a standard SATAii Frame Information Structure that can be sent to any SATA host or device). Therefore, to correctly perform the jitter tests a device specific way to generate the required patterns must be available. We have seen this done on some devices using a serial connection through two wires connected to unlabelled points on the SATA device's PC board. The jitter measurements performed by the SDA do not require these patterns to produce values, the Serial ATA specification requires these patterns so that the values produced are from worst-case patterns and, therefore, have the expected meaning when compared to the specified limits.

Section 6.2.1 Table 5, Receiver specifications

All items in this table are impedances and return loss measurements. Since the SDA does not provide TDR or VNA functionality, our scripts do not automate any of these measurements. Please see the current Serial ATA II: Electrical Specification for more information about these measurements.

Section 6.2.1 Table 6, Lab-Sourced Signal (for Receiver Tolerance Testing)

In general, all receiver tests involve measuring the stimulus from controllable source and setting the source to required limits, and then connecting the source to a SATA device and verifying the error rate. The error rate can be verified using a LeCroy SA Trainer or SAS Trainer, as mentioned above under Frame Error Rate. Our scripts, which control a LeCroy SDA, do not automate these tests. Please see the current Serial ATA II: Electrical Specification for more information about these measurements.

Almost all the items specified for receiver tolerance testing correspond to items tested for Table 4, Transmitted Signal Requirements, but with wider limits. The intent is to require a receiver to handle a signal degraded from the limits that a transmitter is required to meet.

From section 6.2.1 Table 7, OOB Specifications

Our scripts do not automate OOB measurements. However, there are scope setup files (*.lss) and SASTracer generation files (*.ssg) included for conducting OOB tests. Details on using these files are in the MOI in the section on Group 5 tests. Below we will describe how to perform these tests using a LeCroy SDA if some description beyond the text from the specification may be useful.

- **Vthresh (OOB signal detection threshold)**

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
V_{thresh}, OOB Signal Detection Threshold	mVppd	Min	50		120	75		120	6.2.2.6.1	6.4.20
		Nom	100		-	125		-		
		Max	200		240	200		240		

6.2.2.6.1 says:

> "Differential signal amplitude detected as activity by the squelch detector during OOB signaling. V_{diffRX} signals less than the minimum V_{thresh} defined in Table 7 shall not be detected as activity. Signal levels greater than the maximum V_{thresh} defined in Table 7 shall be detected as activity."

6.4.20 says:

> "6.4.20 Squelch Detector Tests
>
> The squelch detector is an essential function in receiving OOB signaling. There are two conditions to test: when above the maximum threshold the detector shall detect, and when below the minimum threshold the detector shall not detect. Figure 72 shows the test setup to set the proper level of the OOB signal. Note the same method is used to calibrate the Lab-Sourced signal amplitude as in section 6.4.5. To ensure the proper detection, multiple tests must be done and the statistics of the results presented to show compliance.
>
> Note: the pattern content in the OOB can affect the detection. The timing of the gaps in the OOB bursts shall be varied to ensure compliance to the OOB timing specification (see Table 7)."

Section 6.4.5 and Figure 73 show connecting a signal source to the HBWS to adjust amplitude, then connecting it using the same cables to a receiver under test.

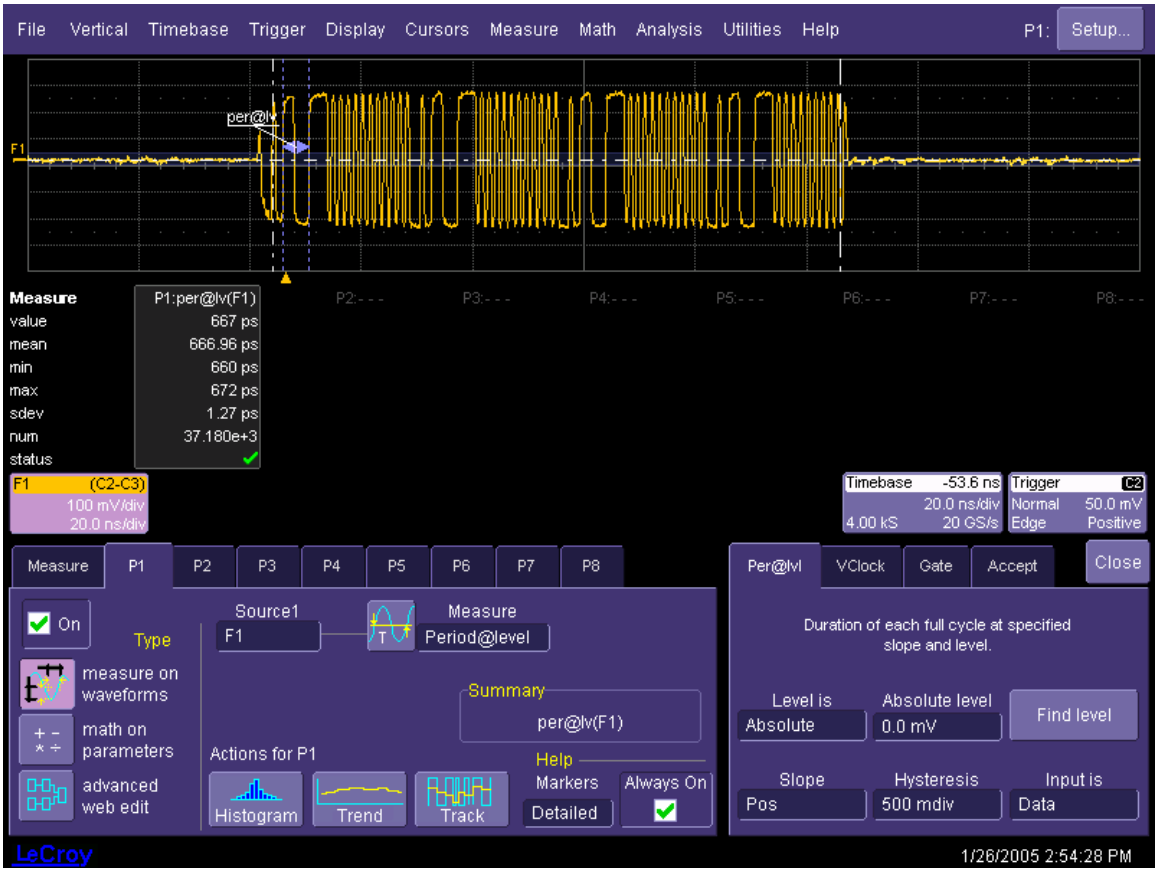
- **UI_{OOB}**

UI_{OOB}, UI During OOB Signaling	ps	Min	646.67	646.67	6.2.2.6.2	-
		Nom	666.67	666.67		
		Max	686.67	686.67		

6.2.2.6.2 says:

> "Operating data period during OOB burst transmission (at Gen1 rate +/- 3%)."

Note that there is no measurement methodology specified. Also, the tolerance is broad. This can easily be measured as min, mean and max statistics of Period@level on data at 1.5 Gb/s expected rate. See the picture and details below.



Math function F1 forms the differential signal as TX+ - TX- (that is C2 - C3).

Note that the sample rate is 20 GS/s. The trigger is on C2 at 50 mV, to trigger on an OOB burst, with a holdoff of 120 ns so it always triggers at the start of an OOB burst.

We measure Period@level of F1. The threshold level should be set to 0.0 V, and the Input type must be set to "Data," as shown above. On the Gate tab, set the Measure Gate to be within the OOB burst; in the picture above the Gate Start is set to 2.20 div and Stop is set to 7.3 div. On the Vclock tab, set the Reference to Custom, and set the "Custom freq." to 1.5 GHz.

In the figure above, the statistics have been accumulated over multiple sweeps. Period@level's markers label the first interval measured in the displayed sweep, all intervals between the Gate Start and Stop settings are measured in each sweep. In the figure, over 37000 intervals have been measured: num shows the number of values accumulated in the statistics. The mean UI_{OOB} is 666.96 ps, max is 672 ps, and min is 660 ps. The device that produced these OOB bursts easily passes the UI_{OOB} test, every interval measured was well within the limits.

- **OOB burst and gap lengths**

COMINIT/ COMRESET and COMWAKE Transmit Burst Length	UI_{OOB}		160	160	6.2.2.6.3	6.4.21
COMINT/ COMRESET Transmit Gap Length	UI_{OOB}		480	480	6.2.2.6.4	6.4.21
COMWAKE Transmit Gap Length	UI_{OOB}		160	160	6.2.2.6.5	6.4.21

6.2.2.6.3 says, in its entirety:

> "Burst length in terms of UI_{OOB} as measured from 100 mV differential crosspoints of first and last edges of a burst."

6.2.2.6.4 and 6.2.2.6.5 both say, in their entirety:

> "Gap length in terms of UI_{OOB} as measured from 100 mV differential crosspoints of last and first edges of bursts."

All have the same measurement methodology reference: 6.4.21

6.4.21 OOB Signaling Tests

Out-of-band signaling is used to signal specific actions during conditions where the receiving interface is in an active mode, a low interface power state, or a test mode.

This section specifies the set of test requirements to ensure that the OOB detector circuits will comply with the OOB signaling sequences under various conditions.

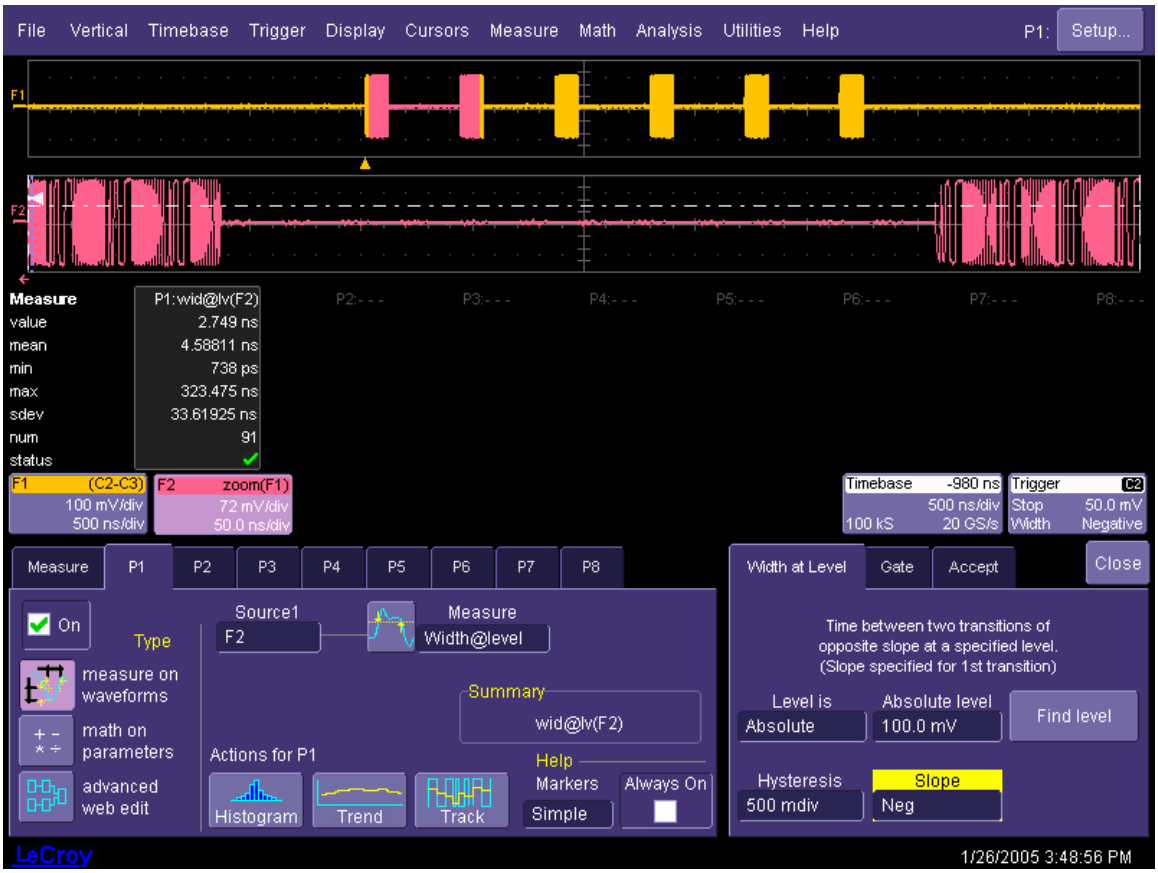
6.4.21 has several subsections concerned not with measuring a number of UI_{OOB} but with making sure that the reaction to a valid OOB sequence after power on and in low power states, etc. is correct. Use the LeCroy SDA's smart trigger to reliably trigger on the first OOB burst. For example, in the Trigger setup dialog, select **C2** as the source, **Width** trigger, **Negative** slope (below 50 mV **Level**), for **Greater Than** 3 µs. The SDA will reliably trigger at the start of the first OOB burst in a sequence of bursts. Acquire a long enough sweep to capture the whole OOB sequence.

Then, to measure the burst length, zoom in on each burst and measure the transmit burst length (same for all three OOB sequences). The burst length can be measured either with cursors or with parameters. Using cursors, be sure to place the cursors at the first and last times at which the differential signal (F1) is at 100 mV. Alternatively, use two Time@level parameters; set the level to 100 mV; set the slopes appropriately (Pos for the first edge and Neg for the last edge) and use the measure Gate to isolate the first edge that passes 100 mV for one of them, and isolate the last edge that crosses 100 mV for the other. The difference between their readings is the burst length.

The transmit gap length can be measured using the **Width@level** parameter, as shown in the figure below. Set "Level is" to **Absolute**, set the level to 100 mV; and set the slope to **Neg**. The measure Gate can be left at default settings (0 to 10 divisions). If Statistics are not on, turn them on from the **Measure** drop-down menu. As shown in the figure below, the longest interval during which the differential signal is below 100 mV is the gap between the bursts. This can be read directly from the max value of the statistics. In the figure, it is 323.475 ns.

> 323.475 ns / 480 UI_{OOB} = 673.906 ps per UI_{OOB}

That is well within the spec for UI_{OOB}, so this test is passed.



Measurements must be correct for each burst and gap.

Note that max width / 480 = 673.906 ps is slightly longer than the mean UI_{OOB} measured from this device. It is not the intent of this test that the gap / measured UI_{OOB} be exactly 480; that would require infinite accuracy of both the device and the measuring system.

In this case, 323.475 ns / measured mean UI_{OOB} (666.96 ps) = 485 UI_{OOB}. Note that the limits on the gap that a receiver must detect (shown in the next test) are substantially wider than the appropriate multiples of the limits of UI_{OOB}: i.e., 646.67 ps * 480 = 310.402 ns, and 686.67 ps * 480 = 329.602 ns; but the "shall detect" limits on COMINIT's gaps are 304 to 336 ns (and the "may detect" limits are far wider). Checking that the gap width divided by the expected number of UI_{OOB} is within the limits for UI_{OOB} is the proper interpretation of the intent of this test.

- **6, 7) OOB sequence gap detection windows (=range requirements)**

COMWAKE Gap Detection Windows	ns	May detect	55 ≤ T < 175	55 ≤ T < 175	6.2.2.6.6	6.4.21
		Shall detect	101.3 ≤ T ≤ 112	101.3 ≤ T ≤ 112		
		Shall not detect	T < 55 or T ≥175	T < 55 or T ≥175		
COMINIT/ COMRESET Gap Detection Windows	ns	May detect	175 ≤ T < 525	175 ≤ T < 525	6.2.2.6.7	6.4.21
		Shall detect	304 ≤ T ≤ 336	304 ≤ T ≤ 336		
		Shall not detect	T < 175 or T ≥ 525	T < 175 or T ≥ 525		

6.2.2.6.6 and 6.2.2.6.7 say basically the same thing: 6.2.2.6.6 is for COMWAKE and 6.2.2.6.7 is identical except each occurrence of the string "COMWAKE" is replaced by the string "COMINIT or COMRESET". Here is 6.2.2.6.6:

> Three timing ranges defining the validation and invalidation of COMWAKE gaps, see Table 7.

Any OOB gap between bursts falling in the defined “May detect” range may be recognized as a valid COMWAKE gap.

Any OOB gap between bursts falling in the “Shall detect” range shall be recognized as a valid COMWAKE gap.

Any OOB gap between bursts falling in the “shall not detect” ranges shall be recognized as an invalid COMWAKE gap (shall not be recognized as a valid COMWAKE gap).

6.4.21 was referenced for “OOB Burst and Gap Length” above. It implies that the user will have to generate illegal gaps from a Laboratory Signal Source and verify the response of the device in several states.

The LeCroy SDA can be used in adjusting the signal source for these tests. The max of Width@level set up as described for “Transmit Gap Length,” above. Each device must have a way to indicate the state that it is in, if it is a suitable signal, the SDA can display that also.

§ § §